APPLICATION NOTE

Design With PIN Diodes

Introduction

The PIN diode finds wide usage in RF, UHF, and microwave circuits. At these types of frequencies, a PIN diode is fundamentally a device with an impedance controlled by its DC excitation. A unique feature of the PIN diode is its ability to control large amounts of RF power with much lower levels of DC.

This Application Note describes the use of PIN diodes in circuit design.

PIN Diode Fundamentals

The PIN diode is a current-controlled resistor at radio and microwave frequencies. It is a silicon semiconductor diode in which a high-resistivity, intrinsic I region is sandwiched between a P-type and N-type region. When the PIN diode is forward biased, holes and electrons are injected into the I region. These charges do not immediately annihilate each other; instead they stay alive for an average time, called the carrier lifetime, *t*. This results in an average stored charge, *Q*, which lowers the effective resistance of the I region to a value R_S.

When the PIN diode is at zero or reverse bias, there is no stored charge in the I region and the diode appears as a capacitor, C_T, shunted by a parallel resistance R_P.

PIN diodes are described using the following parameters:

- R_S series resistance under forward bias
- C_T total capacitance at zero or reverse bias
- R_D parallel resistance at zero or reverse bias
- V_R maximum allowable DC reverse bias voltage
- τ carrier lifetime
- Θ_{AV} average thermal resistance or:
  - P_D maximum average power dissipation
- Θ_{PULSE} pulse thermal impedance or:
  - P_P maximum peak power dissipation

By varying the I region width and diode area, it is possible to construct PIN diodes of different geometries that result in the same R_S and C_T characteristics. These devices may have similar small signal characteristics. However, the thicker I region diode would have a higher bulk, or R_F breakdown voltage, and better distortion properties. On the other hand, the thinner device would have faster switching speed.

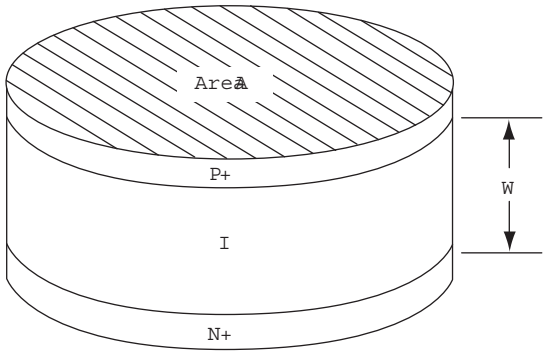


Figure 1. PIN Diode Cross-Section

There is a common misconception that carrier lifetime, τ, is the only parameter that determines the lowest frequency of operation and the distortion produced. This is indeed a factor, but equally important is the thickness of the I region, *W*, which relates to the transit time frequency of the PIN diode.

Low-Frequency Model

At low frequencies (below the transit time frequency of the I region) and DC, the PIN diode behaves like a silicon PN junction semiconductor diode. Its I-V characteristic (see Figure 2) determines the DC voltage at the forward bias current level. PIN diodes are often rated for the forward voltage, V_F, at a fixed DC bias.

The reverse voltage, V_R, rating of a PIN diode is a guarantee from the manufacturer that no more than a specified amount, generally 10 µA, of reverse current is present when V_R is applied. It is not necessarily the avalanche or bulk breakdown voltage, V_B, determined by the I region width (approximately 10 V/mm). PIN diodes of the same bulk breakdown voltage may have different voltage ratings. Generally, the lower the voltage rating, the less expensive the PIN diode.

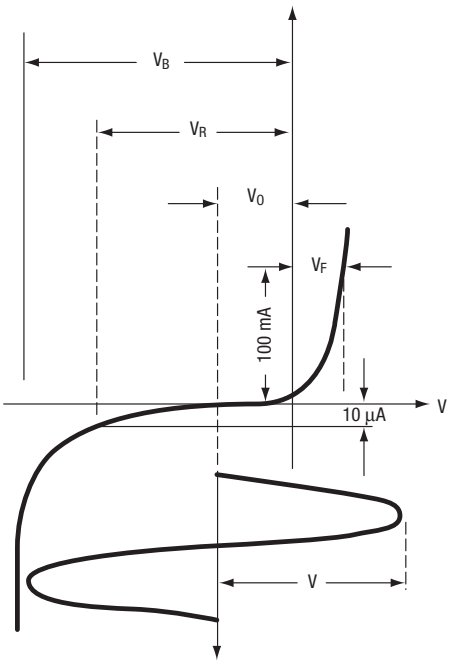


Figure 2. Typical PIN Diode I-V Characteristics

Large Signal Model

When the PIN diode is forward biased, the stored charge, *Q*, must be much greater than the incremental stored charge added or removed by the RF current, I_{RF}. To ensure this, the following inequality must hold:

$$Q >> \frac{I_{RF}}{2\pi f} \tag{1}$$

RF Electrical Modeling of the PIN Diode

Forward Bias Model

$$R_S = \frac{W^2}{(\mu_n + \mu_p) \times Q} (\Omega) \tag{2}$$

Where: $Q = I_F \times \tau$ (in coulombs)
W = I region width
I_F = forward bias current
τ = carrier lifetime
μ_n = electron mobility
μ_p = hole mobility

In commercially available diodes, the parasitic resistance of the diode package and contacts limit the lowest resistance value. The lowest impedance is affected by the parasitic inductance, *L*, which is generally less than 1 nH.

Equation (2) is valid at frequencies higher than the I region transmit time frequency, according to the following relationship:

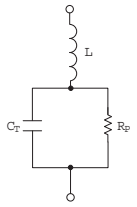
$$f > \frac{1300}{W^2} \text{ (where } f \text{ is in MHz and } W \text{ in } \mu\text{m)} \tag{3}$$

For this equation, it is assumed that the RF signal does not affect the stored charge.

Zero or Reverse Bias Model

$$C_T = \frac{\varepsilon A}{W} \tag{4}$$

Where: ε = dielectric constant of silicon
A = area of diode junction



Equation (4) is valid at frequencies above the dielectric relaxation frequency of the I region, according to the following relationship:

$$f > \frac{1}{2\pi\rho\varepsilon} \text{ (where } \rho \text{ is the resistivity of the I region)} \tag{5}$$

At lower frequencies, the PIN diode acts like a varactor. In these cases, the value R_P is proportional to voltage and inversely proportional to frequency. In most RF applications, its value is higher than the reactance of the capacitance, C_T, and is less significant.

Under reverse bias, the diode should not be biased beyond its DC voltage rating, V_R. The avalanche or bulk breakdown voltage, V_B, of a PIN diode is proportional to the I region width, *W*, and is always higher than V_R.

In a typical application, the maximum negative voltage swing should never exceed V_B. An instantaneous excursion of the RF signal into the positive bias direction generally does not cause the diode to go into conduction because of slow reverse to forward switching speed.

The DC reverse bias needed to maintain low PIN diode conductance has been analyzed[1] and is related to the magnitude of the RF signal and I region width.

Switching Speed Model

The switching speed in any application depends on the driver circuit as well as the PIN diode. Certain primary PIN properties can influence switching speed.

A PIN diode has two switching speeds from forward bias to reverse bias, T_{FR}, and from reverse bias to forward bias, T_{RF}. The diode characteristic that affects T_{FR} is τ, carrier lifetime. The value of T_{FR} may be computed from the forward current, I_F, and the initial reverse current, I_R, as follows (and illustrated in Figure 3):

$$T_{FR} = \tau \log_e \left(1 + \frac{I_F}{I_R} \right) \quad (6)$$

Where T_{FR} is measured in seconds.

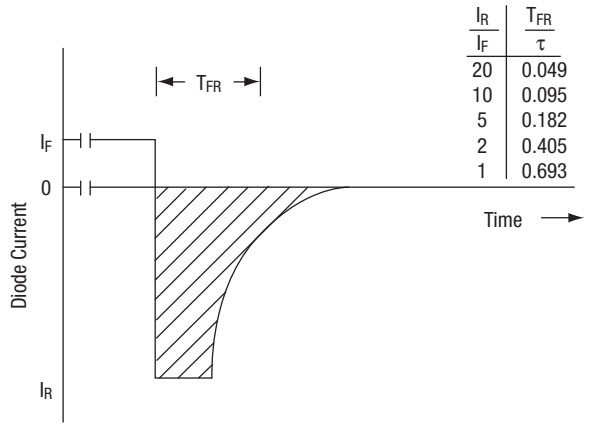


Figure 3. Diode Current vs Time

The reverse bias to forward bias time, T_{RF}, depends primarily on I region width, W, as indicated in the following Table of typical data:

I-Width (µm)	To 10 mA From:		To 50 mA From:		To 100 mA From:	
	10 V (µs)	100 V (µs)	10 V (µs)	100 V (µs)	10 V (µs)	100 V (µs)
175	7.0	5.0	3.0	2.5	2.0	1.5
100	2.5	2.0	1.0	0.8	0.6	0.6
50	0.5	0.4	0.3	0.2	0.2	0.1

Thermal Model

The maximum allowable power dissipation, P_D, is determined by the following equation:

$$P_D = \frac{T_J - T_A}{\theta} \quad (7)$$

Where: P_D = power dissipation in Watts.

T_J = maximum allowable junction temperature (usually 175 °C)

T_A = ambient or heat sink temperature.

Power dissipation may be computed as the product of the RF current squared, multiplied by the diode resistance, R_S.

For Continuous Wave (CW) applications, the value of thermal resistance, Θ, used is the average thermal resistance, Θ_{AV}.

In most pulsed RF and microwave applications where the Duty Factor (DF) is less than 10 percent and the pulse width, T_P, is less than the thermal time constant of the diode, good approximation of the effective value of Θ in Equation (7) may be computed as follows:

$$\Theta = DF \times \Theta_{AV} + \Theta_{TP} \quad (8)$$

Where: Θ = thermal resistance in °C/W.

Θ_{TP} = thermal impedance of the diode for the time interval corresponding to T_P.

Figure 4 indicates how junction temperature is affected during a pulsed RF application.

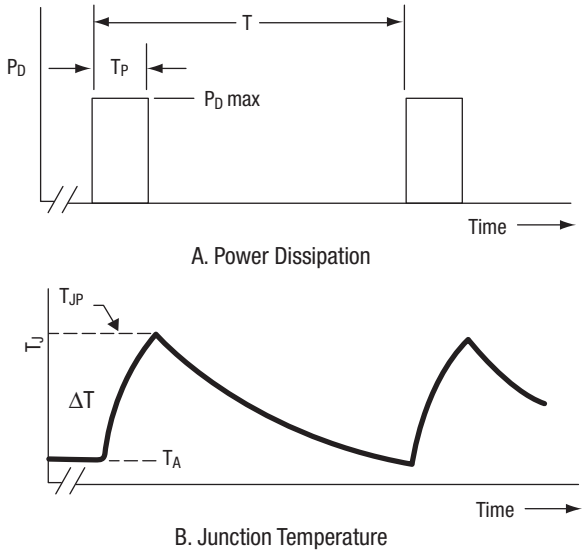


Figure 4. Power Dissipation and Junction Temperature vs Time

PIN Diode Applications

Switches

PIN diodes are commonly used as switching elements to control RF signals. In these applications, the PIN diode can be biased to either a high or low impedance device state, depending on the level of stored charge in the I region.

A simple untuned Single Pole, Single Throw (SPST) switch may be designed using either a single series or shunt connected PIN diode, as shown in Figure 5. The series connected diode switch is commonly used when minimum insertion loss is required over a broad frequency range. This design is also easier to physically realize using printed circuit techniques, since no through holes are required in the circuit board.

When VC1 is biased to 5 V and VC2 is Biased to 0 V, the PIN diode is forward biased and appears as a low impedance to the RF signal.

As current is increased in the forward direction, the value of *Rs* (series resistance) becomes lower and the overall insertion loss of the switch is reduced. When the polarities of VC1 and VC2 are reversed, the PIN diode appears as an open circuit or large resistance with some associated reverse bias capacitance (*CJ*). The insertion loss of the structure becomes high and most of the energy is reflected back towards the RF source, isolation state. So, by its nature this type of switch would be defined as a reflective switch when in the zero or reverse biased state.

This particular bias circuitry offers the ability for the diode to be either forward or reverse biased using a single positive control voltage. A negative control voltage would normally have been required to provide a proper reverse bias on the diode in the isolation state. This technique eliminates the need for this negative voltage while still improving overall device linearity while only using a positive supply voltage.

However, a single shunt mounted diode produces higher isolation values across a wider frequency range and results in a design capable of handling more power since it is easier to heat sink the diode.

Multi-throw switches are more frequently used than single-throw switches. A simple multi-throw switch may be designed that uses a series PIN diode in each arm adjacent to the common port. Improved performance is obtained by using “compound switches,” which are combinations of series and shunt connected PIN diodes, in each arm.

For narrow-band applications, quarter-wave spaced multiple diodes may also be used in various switch designs to obtain improved operation. In the following section, each of these types of switches are discussed in detail and design information is provided to help select PIN diodes and to help predict circuit performance.

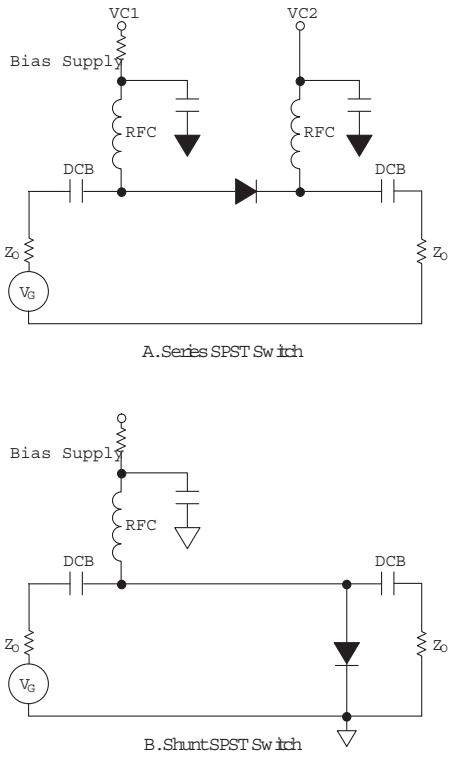


Figure 5. PIN Diode SPST Switches

Series Connected Switch

Figure 6 shows two basic types of PIN diode series switches, a Single-Pole, Single Throw (SPST) and a Single-Pole, Double-Throw (SPDT) switch, commonly used in broadband designs. In both cases, the diode is in a “pass power” condition when it is forward biased and presents a low forward resistance, *Rs*, between the RF generator and load.

For a “stop power” condition, the diode is at zero or reverse bias so that it presents a high impedance between the source and load. In series-connected switches, the maximum isolation obtainable depends primarily on the capacitance of the PIN diode, while the insertion loss and power dissipation are functions of the diode resistance. The principal operating parameters of a series switch can be obtained using the equations shown in the following sections.

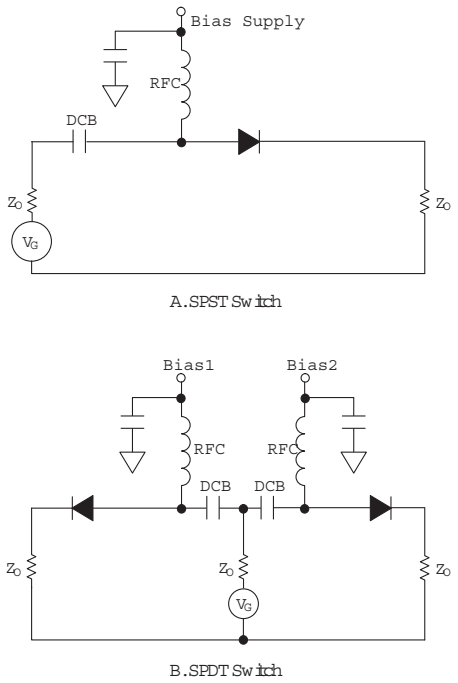


Figure 6. SPST and SPDT Switch Schematics

Insertion Loss (Series Switch)

$$IL = 20\log_{10}\left(1 + \frac{R_S}{2Z_0}\right) \quad (9)$$

Equation (9) computes insertion loss in dB for an SPST series switch. The plot shown in Figure 7 illustrates insertion loss versus resistance for a 50 Ω impedance design. For multi-throw switches, the insertion loss is slightly higher due to any mismatch caused by the capacitance of the PIN diodes in the "off" arms. This additional insertion loss can be determined from Figure 10 after first computing the total shunt capacitance of all "off" arms of the multi-throw switch.

Isolation (Series Switch)

$$Iso = 10\log_{10}\left[1 + (4\pi fCZ_0)^{-2}\right] \quad (10)$$

Equation (10) computes isolation in dB for an SPST diode switch. Add 6 dB for a Single-Pole, No-Throw (SPNT) switch to account for the 50 percent voltage reduction across the "off" diode due to the termination of the generator in its characteristic impedance. The plot shown in Figure 8 illustrates isolation as a function of capacitance for a 50 Ω impedance design.

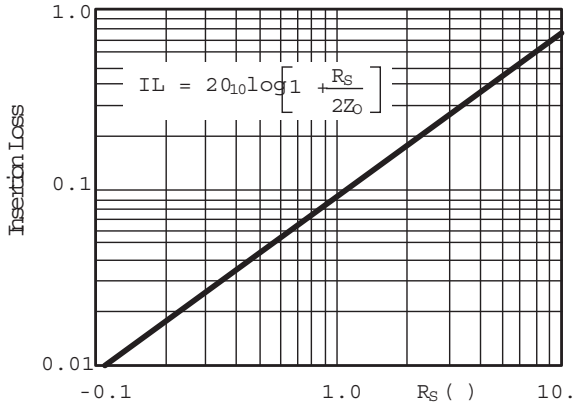


Figure 7. Insertion Loss for PIN Diode Series Switch in a 50 Ω System

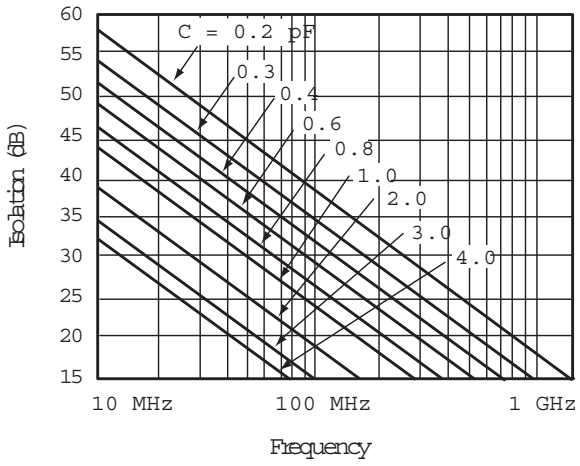


Figure 8. Isolation for an SPST Diode Series Switch in a 50 Ω System (Add 6 dB for Multi-Throw Switches [SPNTs])

Power Dissipation (Series Switch in Forward Bias)

$$P_D = \frac{4R_S Z_0}{(2Z_0 + R_S)^2} \times P_{AV} \quad (11)$$

Where: P_D = power dissipation in Watts

For the condition: Z0 >> Rs, this becomes:

$$P_D = \frac{R_S}{Z_0} \times P_{AV} \quad (12)$$

Where the maximum available power (in Watts) is given by:

$$P_{AV} = \frac{V_G{}^2}{4Z_0} \quad (13)$$

It should be noted that Equations (11) and (12) apply only for perfectly matched switches. For SWR (σ) values other than unity,

multiply these equations by $[2\sigma/(\sigma+1)]^2$ to obtain the maximum required diode power dissipation rating.

Peak Current (Series Switch)

$$I_P = \sqrt{\frac{2P_{AV}}{Z_0}} \times \left(\frac{2\sigma}{\sigma+1}\right) \quad (14)$$

Where I_P = peak current in amps.

In the case of a 50 Ω system, equation (14) reduces to:

$$I_P = \frac{\sqrt{P_{AV}}}{5} \times \left(\frac{2\sigma}{\sigma+1}\right) \quad (15)$$

Peak RF Voltage (Series Switch)

$$V_P = \sqrt{8Z_0P_{AV}} \quad \text{(SPST)}$$

$$V_P = \sqrt{2Z_0P_{AV}} \times \left(\frac{2\sigma}{\sigma+1}\right) \quad \text{(SPNT)} \quad (16)$$

For a 50 Ω system, Equation (16) becomes:

Where V_P = peak voltage in volts.

$$V_P = 20\sqrt{P_{AV}} \quad \text{(SPST)}$$

$$V_P = 10\sqrt{P_{AV}} \times \left(\frac{2\sigma}{\sigma+1}\right) \quad \text{(SPNT)} \quad (17)$$

Shunt Connected Switch

Figure 9 shows two typical shunt-connected PIN diode switches. These shunt diode switches offer high isolation for many applications and, since the diode may be heat sunk at one electrode, it is capable of handling more RF power than a diode in a series type switch.

In shunt switch designs, the isolation and power dissipation are functions of the diode's forward resistance, whereas the insertion loss is primarily dependent on the capacitance of the PIN diode. The principal operating parameters of a shunt switch can be obtained using the equations shown in the following sections.

Insertion Loss (Shunt Switch)

$$IL = 10\log_{10}\left[1 + (\pi f C_T Z_0)^2\right] \quad (18)$$

Equation (18) computes insertion loss in dB for both SPST and SPNT shunt switches. The plot shown in Figure 10 illustrates insertion loss versus frequency for a 50 Ω impedance design.

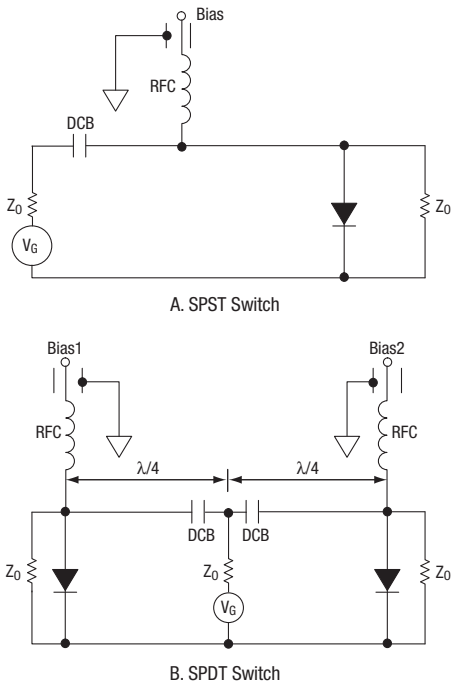


Figure 9. Shunt Connected Switches 2-5

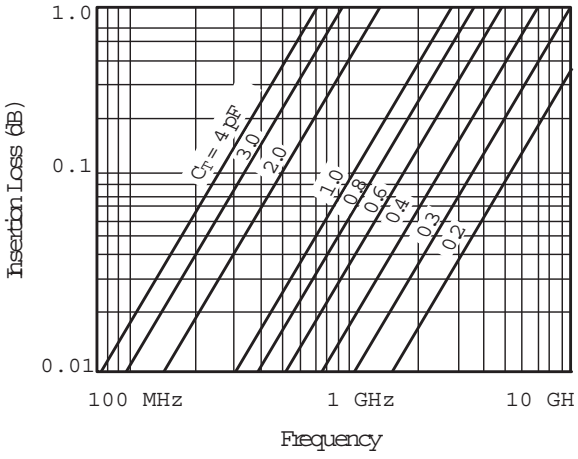


Figure 10. Insertion Loss For a Shunt PIN Switch in a 50 Ω System

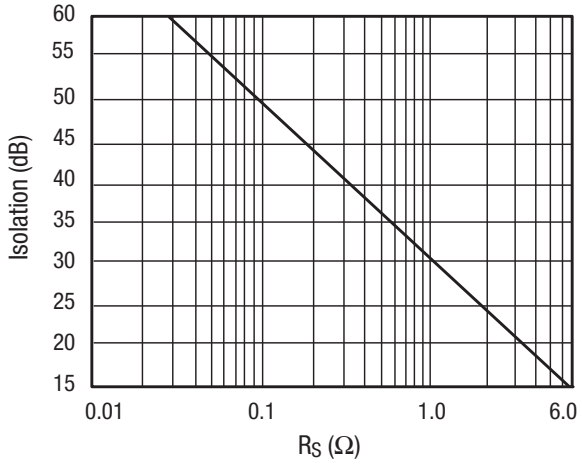


Figure 11. Isolation for SPST Shunt PIN Switches in a 50 Ω System (Add 6 dB for Multi-Throw Switches [SPNTs])

Isolation (Shunt Switch)

$$Iso = 20\log_{10}\left(1 + \frac{Z_0}{2R_S}\right) \quad (19)$$

Equation (19) computes isolation in dB for an SPST shunt switch. Add 6 dB to obtain the correct isolation for a multi-throw switch. The plot shown in Figure 11 illustrates isolation versus resistance for a 50 Ω impedance design.

Power Dissipation (Shunt Switch in Forward Bias)

$$P_D = \frac{4R_S Z_0}{(Z_0 + 2R_S)^2} \times P_{AV} \quad (20)$$

Where P_D = power dissipation in Watts

For the condition: $Z0 >> Rs$, this becomes:

$$P_D = \frac{4R_S}{Z_0} \times P_{AV} \quad (21)$$

Where the maximum available power (in Watts) is given by:

$$P_{AV} = \frac{{V_G}^2}{4Z_0} \quad (22)$$

Power Dissipation (Shunt Switch in Reverse)

$$P_D = \frac{Z_0}{R_P} \times P_{AV} \quad (23)$$

Where P_D = power dissipation in Watts

R_P = parallel resistance of reverse biased diode in Ω

Peak RF Current (Shunt Switch)

$$I_P = \sqrt{\frac{8P_{AV}}{Z_0}} \quad \text{(SPST)}$$

$$I_P = \sqrt{\frac{2P_{AV}}{Z_0}} \times \left(\frac{2\sigma}{\sigma + 1}\right) \quad \text{(SPNT) (24)}$$

Where I_P = peak current in amps.

In the case of a 50 Ω system, Equation (24) reduces to:

$$I_P = 0.4\sqrt{P_{AV}} \quad \text{(SPST)}$$

$$I_P = 0.2\sqrt{P_{AV}} \times \left(\frac{2\sigma}{\sigma + 1}\right) \quad \text{(SPNT) (25)}$$

Peak RF Voltage (Shunt Switch)

$$V_P = \sqrt{2Z_0 P_{AV}} \times \left(\frac{2\sigma}{\sigma + 1}\right) \quad (26)$$

Where V_P = peak voltage in volts.

For a 50 Ω system, Equation (26) becomes:

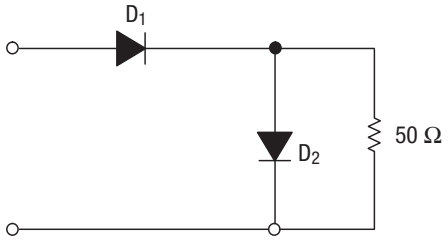
$$V_P = 10\sqrt{P_{AV}} \times \left(\frac{2\sigma}{\sigma + 1}\right) \quad (27)$$

Compound and Tuned Switches

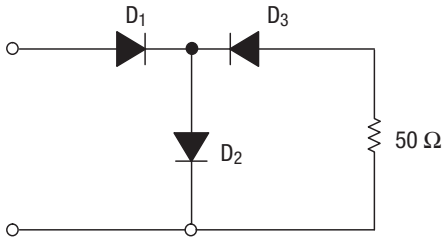
In practice, it is usually difficult to achieve more than 40 dB isolation using a single PIN diode, either in shunt or series, at RF and higher frequencies. The causes of this limitation are generally radiation effects in the transmission medium and inadequate shielding. To overcome this, there are switch designs that use combinations of series and shunt diodes (compound switches), and switches that use resonant structures (tuned switches) affecting improved isolation performance.

The two most common compound switch configurations are PIN diodes mounted in either ELL (series-shunt) or TEE designs, as shown in Figure 12. In the insertion loss state for a compound switch, the series diode is forward biased and the shunt diode is at zero or reverse bias. The reverse is true for the isolation state.

This adds some complexity to the bias circuitry in comparison to simple switches. A summary of formulas used to calculate insertion loss and isolation for compound and simple switches is given in Table 1.



A. ELL (Series-Shunt) SPST Switch



B. TEE SPST Switch

Figure 12. Compound Switches

Figure 13 shows the performance of an ELL type switch, a diode rated at 3.3 pF, maximum capacitance, and 0.25 Ω with *Rs* maximum at 100 mA. In comparison, a simple series connected using the same diode switch would have similar insertion loss to the 100 MHz contour and the isolation would be 15 dB maximum at 100 MHz, falling off at the rate of 6 dB per octave.

A tuned switch may be constructed by spacing two series diodes or two shunt diodes a wavelength apart, as shown in Figure 14. The resulting value of isolation in the tuned switch is twice that obtainable in a single diode switch. The insertion loss of the tuned series switch is higher than that of the simple series switch and may be computed using the sum of the diode resistance as the *Rs* value in Equation (9). In the tuned shunt switch the insertion loss may even be lower than in a simple shunt switch because of a resonant effect of the spaced diode capacitances.

Quarter-wave spacing need not be limited to frequencies where the wavelength is short enough to install a discrete length of line. There is a lumped circuit equivalent that simulates the quarter-wave section and may be used in the RF band. This is shown in Figure 15. These tuned circuit techniques are effective in applications having bandwidths on the order of 10 percent of the center frequency.

Table 1. Summary of Formulas for SPST Switches (Add 6 dB to Isolation to Obtain Value for Single Pole Multi-Throw Switch)

Type	Isolation (dB)	Insertion Loss (dB)
Series	$10\log_{10}\left[1+\left(\frac{X_C}{2Z_0}\right)^2\right]$	$20\log_{10}\left[1+\left(\frac{R_S}{2Z_0}\right)\right]$
Shunt	$20\log_{10}\left[1+\left(\frac{Z_0}{2RS}\right)\right]$	$10\log_{10}\left[1+\left(\frac{Z_0}{2X_C}\right)^2\right]$
Series-Shunt	$10\log_{10}\left[\left(1+\frac{Z_0}{2R_S}\right)^2+\left(\frac{X_C}{2Z_0}\right)^2\left(1+\frac{Z_0}{R_S}\right)^2\right]$	$10\log_{10}\left[\left(1+\frac{R_S}{2Z_0}\right)^2+\left(\frac{Z_0+R_S}{2X_C}\right)^2\right]$
TEE	$10\log_{10}\left[1+\left(\frac{X_C}{Z_0}\right)^2\right]+10\log_{10}\left[\left(1+\frac{Z_0}{2R_S}\right)^2+\left(\frac{X_C}{2R_S}\right)^2\right]$	$20\log_{10}\left(1+\frac{R_S}{Z_0}\right)+10\log_{10}\left[1+\left(\frac{Z_0+R_S}{2X_C}\right)^2\right]$

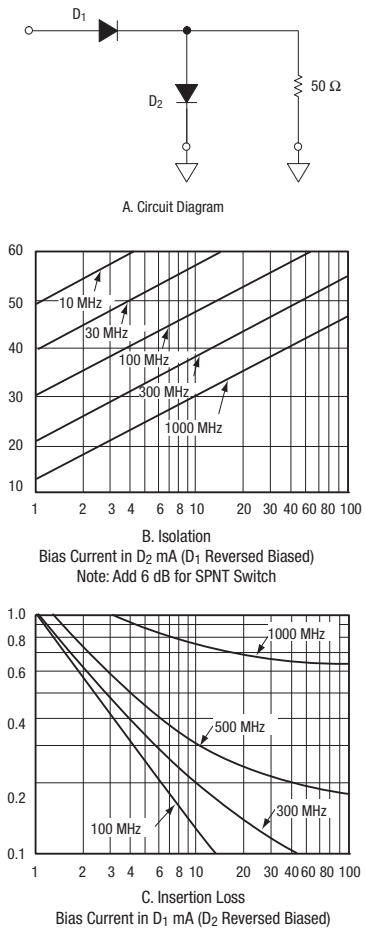


Figure 13. Series Shunt Switch

Transmit/Receive Switches

There is a class of switches used in transceiver applications whose function is to connect the antenna to the transmitter (exciter) in the transmit state and to the receiver during the receiver state. When PIN diodes are used as elements in these switches, they offer higher reliability, better mechanical ruggedness, and faster switching speed than electro-mechanical designs.

The basic circuit for an electronic switch consists of a PIN diode connected in series with the transmitter, and a shunt diode connected a quarter wavelength away from the antenna node. A lumped-component equivalent of a quarter-wave transmission line is shown in Figure 15.

When switched into the transmit state, each diode becomes forward biased. The series diode appears as a low impedance to the signal heading toward the antenna, and the shunt diode effectively shorts the antenna terminals of the receiver to prevent overloading.

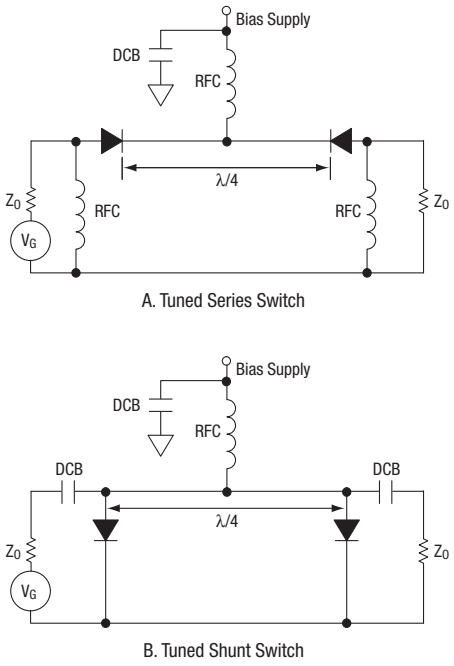


Figure 14. Tuned SPDT Switch in Series and Shunt Configuration

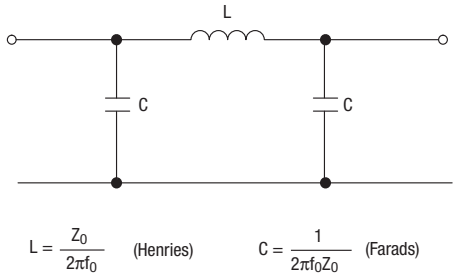


Figure 15. Quarter-Wave Line Equivalent

Transmitter insertion loss and receiver isolation depend on the diode resistance. If R_S is 1 Ω greater than 30 dB isolation and less than 0.2 dB insertion, loss can be expected. This performance is achievable over a 10 percent bandwidth.

In the receive condition, the diodes are at zero or reverse bias and present essentially a low capacitance, C_T, which creates a direct low insertion loss path between the antenna and receiver. The off transmitter is isolated from this path by the high impedance series diode.

The amount of power, P_A, that this switch can handle depends on the power rating of the PIN diode, P_D, and the diode resistance. Equation 28 shows this relationship for an antenna maximum SWR of σ.

$$P_A = \frac{P_D Z_0}{R_S}\left(\frac{\sigma + 1}{2\sigma}\right)^2 \quad (28)$$

Where the amount of power, P_A, is in Watts.

In a 50 system where the condition of a totally mismatched antenna must be considered, this equation becomes:

$$P_A = \frac{12.5 \times P_D}{R_S} \quad (29)$$

Skyworks SMP1322-011LF is a surface mount PIN diode rated at 0.25 W dissipation to a 25 °C contact. The resistance of this diode is 0.50 Ω (max) at 10 mA. A quarter-wave switch using the SMP1322-011LF may then be computed to handle 6.25 W with a totally mismatched antenna.

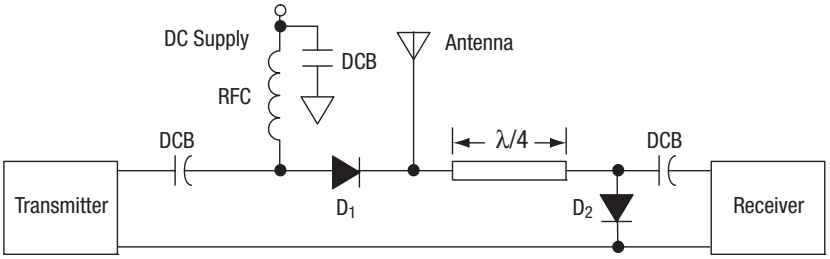
It should be pointed out that the shunt diode of the quarter-wave antenna switch dissipates about as much power as the series diode. This may not be apparent from Figure 16. However, it can be shown that the RF current in both the series and shunt diode is practically identical.

Broadband antenna switches using PIN diodes may be designed using the series connected diode circuit shown in Figure 17. The frequency limitation of this switch results primarily from the capacitance of D2.

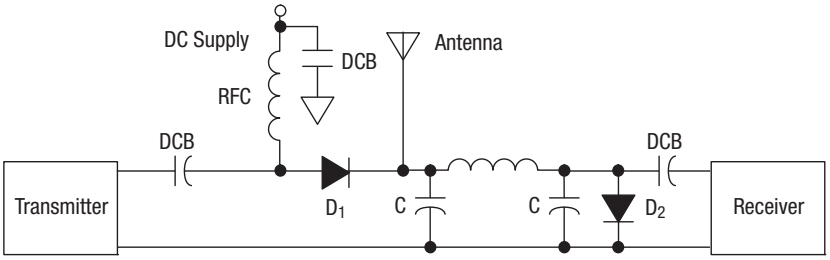
In this case, forward bias is applied either to D1 during the transmit or D2 during receive. In high power applications (> 5 W), it is often necessary to apply reverse voltage on D2 during transmit. This may be accomplished either by a negative polarity power supply at Bias 2, or by having the forward bias current of D1 flow through resistor R to apply the required negative voltage.

The selection of diode D1 is based primarily on its power handling capability. It need not have a high voltage rating since it is always forward biased in its low resistance state when high RF power is applied. Diode D2 does not pass high RF current but must be able to hold off the RF voltage generated by the transmitter. It is primarily selected on the basis of its capacitance, which determines the upper frequency limit and its ability to operate at low distortion.

Using the SMP1322-011LF as D1, and an SMP1302-001LF or SOT-23 PIN diode that are rated at 0.3 pF max as D2, greater than 25 dB receiver isolation may be achieved up to 400 MHz. The expected transmit and receive insertion loss with the PIN diodes biased at 10 mA are 0.1 dB and 0.3 dB, respectively. This switch can handle RF power levels up to 6.25 W.



A. Antenna Switch Using λ/4 Line Length



B. Antenna Switch Using Discrete Components

Figure 16. Quarter-Wave Antenna Switches

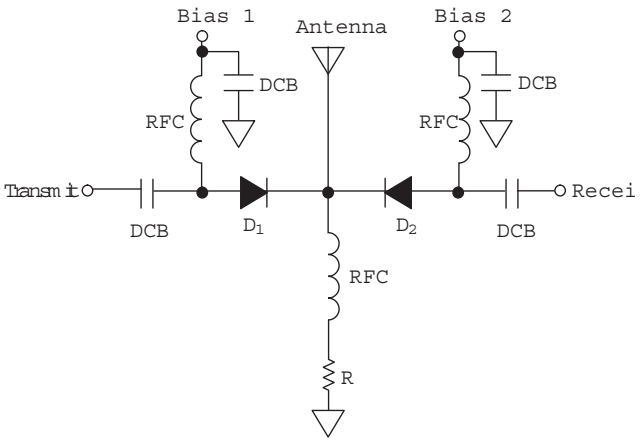


Figure 17. Broadband Antenna Switch

Practical Design Hints

PIN diode circuit performance at RF frequencies is predictable and should conform closely to the design equations. When a switch is not performing satisfactorily, the fault is often not due to the PIN diode but to other circuit limitations such as circuit loss, bias circuit interaction, or lead length problems (primarily when shunt PIN diodes are used).

It is good practice in a new design to first evaluate the circuit loss by substituting, alternatively, a wire short or open in place of the PIN diode. This simulates the circuit performance with "ideal PIN diodes." Any deficiency in the external circuit may then be corrected before inserting the PIN diodes.

PIN Diode Attenuators

In an attenuator application, the resistance characteristic of the PIN diode is exploited not only at its extreme high and low values, as in switches, but at the finite values in between.

The resistance characteristic of a PIN diode when forward biased to IF1 depends on the I region width (W) carrier lifetime (ττ), and the hole and electron mobilities (μp, μn) as follows:

$$R_S = \frac{W^2}{[(\mu_P + \mu_n)I_F\tau]} \qquad (30)$$

Where the PIN diode resistance, *Rs*, is in Ω.

For a PIN diode with an I region width of typically 250 mm, a carrier lifetime of 4 ms, μn of 0.13, μp of 0.05 $m^2/v \times s$, Figure 18 shows the *Rs* versus current characteristic.

When a PIN diode for an attenuator application is selected, the designer must often be concerned about the range of diode resistance, which defines the dynamic range of the attenuator.

PIN diode attenuators tend to be more distortion sensitive than switches since their operating bias point often occurs at a low value of quiescent stored charge. A thin I region PIN operates at lower forward bias currents than thick PIN diodes, but the thicker one generates less distortion.

PIN diode attenuator circuits are used extensively in Automatic Gain Control (AGC) and RF leveling applications, as well as in electronically controlled attenuators and modulators. A typical configuration of an AGC application is shown in Figure 19. The PIN diode attenuator may take many forms ranging from a simple series or shunt mounted diode acting as a lossy reflective switch, or a more complex structure that maintains a constant matched input impedance across the full dynamic range of the attenuator.

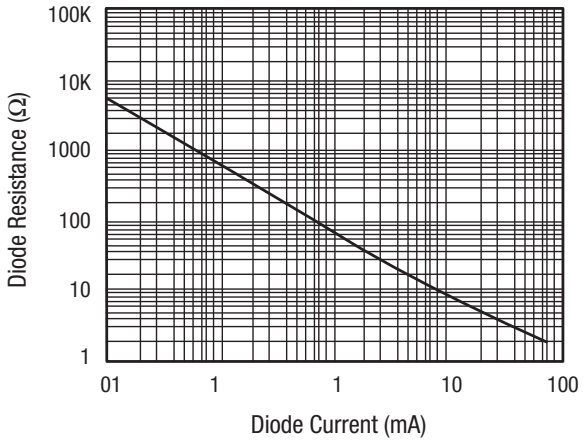


Figure 18. Typical Diode Resistance vs Forward Current

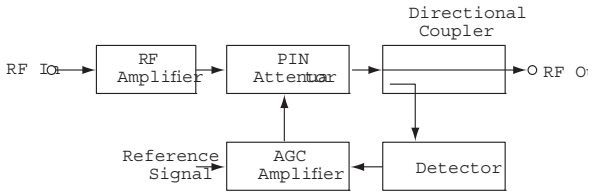


Figure 19. RF AGC/Leveler Circuit

Although there are other methods that provide AGC functions, such as varying the gain of the RF transistor amplifier, the PIN diode approach generally results in lower power drain, less frequency pulling, and lower RF signal distortion. The latter results are especially true when diodes with thick I regions and long carrier lifetimes are used in the attenuator circuits. Using these PIN diodes, one can achieve wide dynamic range attenuation with low signal distortion at frequencies ranging from below 1 MHz up to well over 1 GHz.

Reflective Attenuators

An attenuator may be designed using single series or shunt connected PIN diode switch configurations, as shown in Figure 20. These attenuator circuits use the current-controlled resistance characteristic of the PIN diode, not only in its low loss states (very high or low resistance), but also at in-between, finite resistance values.

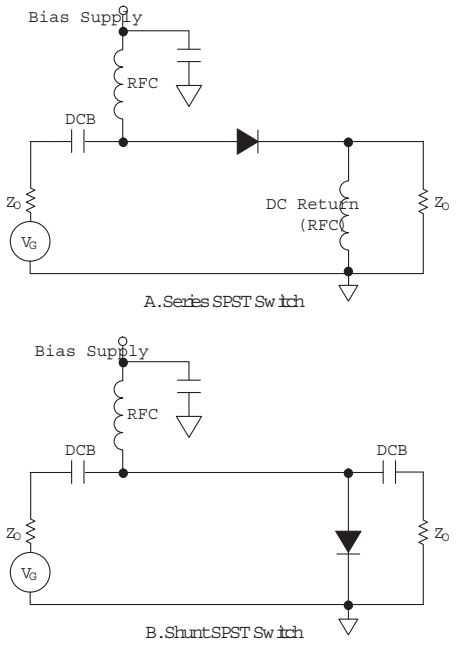


Figure 20. SPST PIN Diode Switches

The attenuation value obtained using these circuits can be computed from Equations (31) and (32).

Attenuation (in dB) of series-connected PIN diode attenuators:

$$A = 20\log\left(1 + \frac{R_S}{2Z_0}\right) \quad (31)$$

Attenuation of shunt-connected PIN diode attenuators:

$$A = 20\log\left(1 + \frac{Z_0}{2R_S}\right) \quad (32)$$

These equations assume the PIN diode to be purely resistive. The reactance of the PIN diode capacitance, however, must also be taken into account at frequencies at which its value begins to approach the PIN diode resistance value.

Matched Attenuators

Attenuators built from switch design are basically reflective devices that attenuate the signal by producing a mismatch between the source and the load. Matched PIN diode attenuator designs, which exhibit constant input impedance across the entire attenuation range, are also available. They use either multiple PIN diodes biased at different resistance points or bandwidth limited circuits using tuned elements.

Quadrature Hybrid Attenuators

Although a matched PIN attenuator may be achieved by combining a ferrite circulator with one of the previous simple reflective devices, the more common approach makes use of quadrature hybrid circuits.

Quadrature hybrids are commonly available at frequencies from below 10 MHz to above 1 GHz, with bandwidth coverage often exceeding a decade. Figures 21 and 22 show typical quadrature hybrid circuits that use series and shunt connected PIN diodes. Equations (33) and (34) summarize this performance.

Quadrature hybrid (series-connected PIN diodes):

$$A = 20\log\left(1 + \frac{2Z_0}{R_S}\right) \quad (33)$$

Quadrature hybrid (shunt-connected PIN diodes):

$$A = 20\log\left(1 + \frac{2R_S}{Z_0}\right) \quad (34)$$

The quadrature hybrid design approach is superior to the circulator coupled attenuator from the standpoint of lower cost and lower frequency operation. Because the incident power is divided into two paths, the quadrature hybrid configuration is also capable of handling twice the power, and this occurs at the 6 dB attenuation point. Each load resistor, however, must be capable of dissipating one-half the total input power at the time of maximum attenuation.

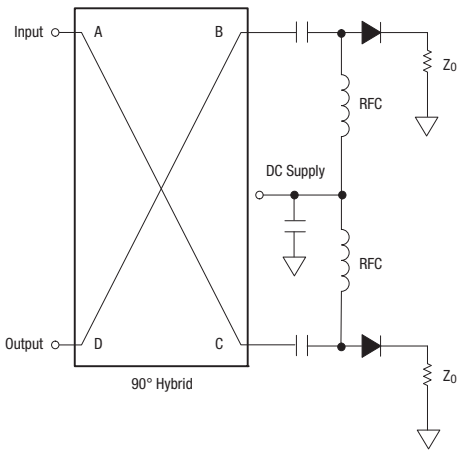


Figure 21. Quadrature Matched Hybrid Attenuator (Series-Connected Diodes)

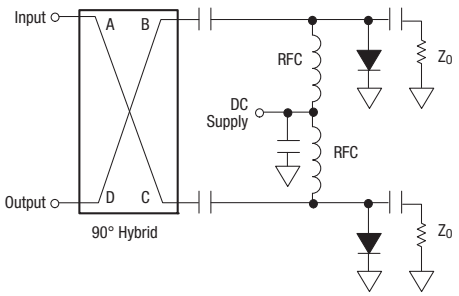


Figure 22. Quadrature Hybrid Matched Attenuator (Shunt-Connected Diodes)

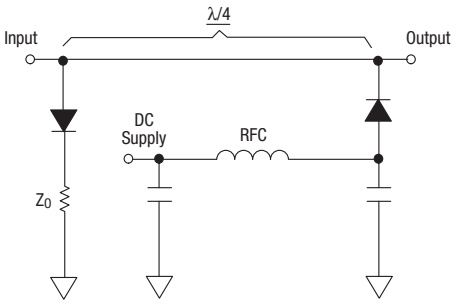


Figure 23. Quarter-Wave Matched Attenuator (Series-Connected Diodes)

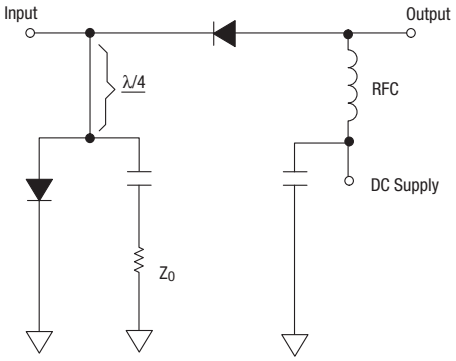


Figure 24. Quarter-Wave Matched Attenuator (Shunt-Connected Diodes)

Both of the above types of hybrid attenuators offer good dynamic range. The series-connected diode configuration is, however, recommended for attenuators used primarily at high attenuation levels (greater than 6 dB), while the shunt mounted diode configuration is better suited for low attenuation ranges.

In a constant impedance attenuator circuit, the power incident on port A divides equally between ports B and C; port D is isolated. The mismatch produced by the PIN diode resistance in parallel with the load resistance at ports B and C reflects part of the power. The reflected power exits port D, isolating port A. Therefore, port A appears matched to the input signal.

Quadrature hybrid attenuators may also be constructed without the load resistor attached in series or parallel to the PIN diode. In these circuits, the forward current is increased from the 50 Ω, maximum attenuation/*Rs* value to lower resistance values. This results in an increased stored charge as the attenuation is lowered, which is desirable for lower distortion.

The purpose of the load resistor is to make the attenuator less sensitive to individual diode differences and to increase the power-handling capacity by a factor of two.

Quarter-Wave Attenuators

An attenuator matched at the input may also be built using quarter-wave techniques. Figures 23 and 24 show examples of these circuits. For the quarter-wave section, a lumped equivalent may be used at frequencies too low for practical use of line lengths. This equivalent is shown in Figure 25.

Attenuation (in dB) for these circuits is calculated according to Equations (35) and (36).

$$A = 20\log\left(1 + \frac{Z_0}{R_S}\right) \quad (35)$$

$$A = 20\log\left(1 + \frac{R_S}{Z_0}\right) \quad (36)$$

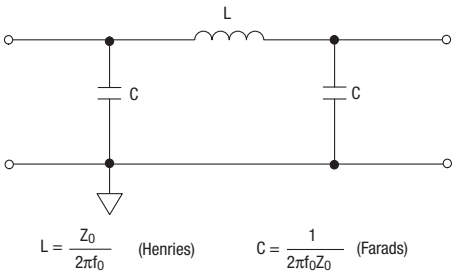


Figure 25. Lumped Circuit Equivalent of Quarter-Wave Line

A matched condition is achieved in these circuits when both diodes are at the same resistance. This condition should normally occur when similar diodes are used, since they are DC series connected, with the same forward bias current flowing through each diode. The series circuit of Figure 23 is recommended for use at high attenuation levels, while the shunt diode circuit of Figure 24 is better suited for low attenuation circuits.

Bridged TEE and PI Attenuators

Attenuator designs using multiple PIN diodes are used for matched broadband applications, especially those covering the low RF (1 MHz) through UHF frequency range. The bridged TEE and PI circuits shown in Figures 26 and 27 are commonly used for these applications.

The attenuation obtained using abridged TEE circuits can be calculated from the following equation:

$$A = 20\,log\left(1 + \frac{Z_0}{R_{S1}}\right) \quad (37)$$

Where: $Z_0{}^2 = R_{S1} \times R_{S2}$ in Ω^2

The relationship between the forward resistance of the two diodes ensures maintenance of a matched circuit at all attenuation values.

The expressions for attenuation and matching conditions for the PI attenuator are given by the following relationships:

$$A = 20\,log\left(\frac{R_{S1} + Z_0}{R_{S1} - Z_0}\right) \quad (38)$$

Where attenuation is measured in dB and series resistance measured in Ohms as follows:

$$R_{S3} = \frac{2R_{S1}Z_0{}^2}{R_{S1}{}^2 - Z_0{}^2} \quad (39)$$

$$R_{S1} = R_{S2}$$

Using these expressions, Figure 28 illustrates the relationship between diode resistance values for a 50 Ω PI attenuator. Note that the minimum value for RS1 and RS2 is 50 Ω. In both the bridged TEE and PI attenuators, the PIN diodes are biased at two different resistance points simultaneously, which must track to achieve proper attenuator performance.

PIN Diode Modulators

PIN diode switches and attenuators may be used as RF amplitude modulators. Square wave or pulse modulation use PIN diode switch designs, whereas linear modulators use attenuator designs.

The design of high-power or distortion-sensitive modulator applications follows the same guidelines as the switch and attenuator counterparts. The PIN diodes used should have thick I regions. Series connected, or, preferably, back-to-back configurations always reduce distortion. The sacrifice in using these devices will be lower maximum frequencies and higher modulation current requirements.

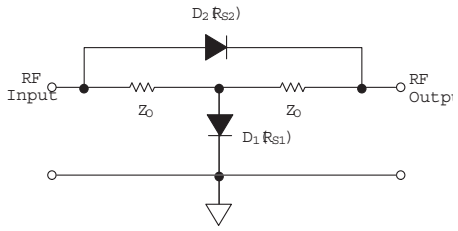


Figure 26. Bridged TEE Attenuator

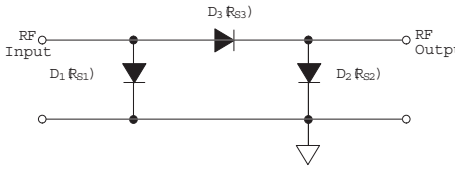


Figure 27. PI Attenuator
(The π and TEE are Broadband Matched Attenuator Circuits)

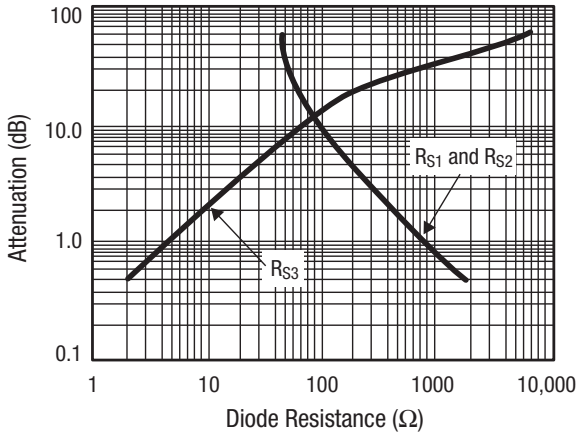


Figure 28. Attenuation of PI Attenuators

The quadrature hybrid design is recommended as a building block for PIN diode modulators. Its inherent built-in isolation minimizes pulling and undesired phase modulation on the driving source.

PIN Diode Phase Shifters

PIN diodes are used as series or shunt connected switches in phase shifter circuit designs. In such cases, the elements switched are either lengths of transmission line or reactive elements.

The criteria for choosing PIN diodes for use in phase shifters is similar to the criteria used to select diodes for other switching applications. One additional factor, however, that must often be considered is the possibility of introducing phase distortion, particularly at high RF power levels or low reverse bias voltages.

Of significant note is the fact that the properties inherent in PIN diodes that yield low distortion (i.e., a long carrier lifetime and thick I regions) also result in low phase distortion of the RF signal.

Three of the most common types of semiconductor phase shifter circuits are the switched line, loaded line, and reflective.

Switched Line Phase Shifter

A basic example of a switched line phase shifter circuit is shown in Figure 29. In this design, two SPDT switches with PIN diodes are used to change the electrical length of a transmission line by some length, $\Delta\ell$. The phase shift obtained from this circuit varies with frequency and is a direct function of this differential line length:

$$\Delta\theta = \frac{2\pi\Delta\ell}{\lambda} \tag{40}$$

Where the phase shift is measured in radians.

The switched line phase shifter is inherently a broadband circuit producing true time delay, with the actual phase shift dependent only on $\Delta\ell$. Because of PIN diode capacitance limitations, this design is most frequently used at frequencies below 1 GHz.

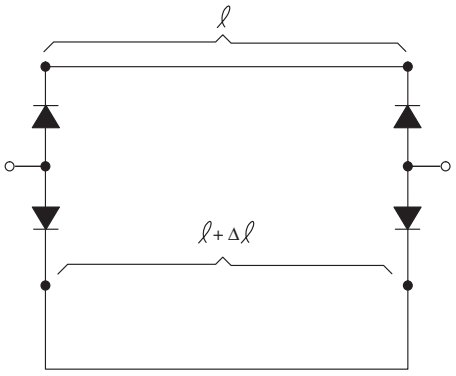


Figure 29. Switched Line Phase Shifter

The power capabilities and loss characteristics of the switched line phase shifter are the same as those of a series connected SPDT switch. A unique characteristic of this circuit is that the power and voltage stress on each diode is independent of the amount of differential phase shift produced by each phase shifter. Therefore, four diodes are required for each bit, with all diodes having the same power and voltage ratings.

Loaded Line Phase Shifter

The loaded line shifter design shown in Figure 30 operates on a different principle than the switched line phase shifter. In this design, the desired maximum phase skirt is divided into several smaller phase shift sections, each containing a pair of PIN diodes that do not completely perturbate the main transmission line.

A major advantage of this phase shifter is its extremely high power capability, due partly to the use of shunt mounted diodes, and the fact that the PIN diodes are never in the direct path of the full RF power.

In loaded line phase shifters, a normalized susceptance, *Bn*, is switched in and out of the transmission path by the PIN diodes. Typical circuits use values of *Bn* much less than unity, resulting in considerable decoupling of the transmitted RF power from the PIN diode. The phase shift for a single section is given by the following equation:

$$\theta = 2\tan^{-1}\left(\frac{Bn}{1-\frac{Bn^2}{8}}\right) \tag{41}$$

Where the phase shift is measured in radians.

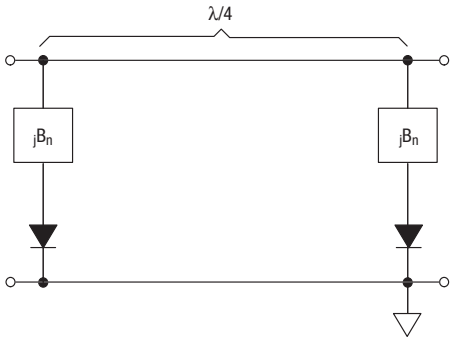


Figure 30. Loaded Line Phase Shifter

The maximum phase shift obtainable from a loaded line section is limited by both bandwidth and diode power handling considerations. The power constraint on obtainable phase shift is shown by the following relationship:

$$\theta\ max = 2\ tan^{-1}\left(\frac{V_{BR} I_F}{4 P_L}\right) \quad (42)$$

Where: $\theta\ max$ = maximum phase angle in radians
P_L = transmitted power
V_{BR} = diode breakdown voltage
I_F = diode current rating

These factors limit the maximum phase shift angle in practical circuits to about 45°. Therefore, a 180° phase shift would require the use of four 45° phase shift sections in its design.

Reflective Phase Shifter

A circuit design that handles both high RF power and large incremental phase shifts with the fewest number of diodes is the hybrid coupled phase shifter shown in Figure 31.

The voltage stress on the shunt PIN diode in this circuit also depends on the amount of desired phase shift, or "bit" size. The greatest voltage stress is associated with the 180° bit and is reduced by the factor $(\sin\theta/2)^{1/2}$ for other bit sizes. The relationship between maximum phase shift, transmitted power, and PIN diode ratings is shown by the following equation:

$$\theta\ max = 2\ sin^{-1}\left(\frac{V_{BR} I_F}{8 P_L}\right) \quad (43)$$

Where the maximum phase shift is measured in radians.

In comparison to the loaded line phase shifter, the hybrid design can handle up to twice the peak power when the same diodes are used.

In both hybrid and loaded line designs, the power dependency of the maximum bit size relates to the product of the maximum RF current and peak RF voltage the PIN diodes can handle.

If the nominal impedance in the plane of the PIN diode is carefully chosen, the current and voltage stress can usually be adjusted to be within the device ratings. In general, this implies lowering the nominal impedance to reduce the voltage stress in favor of higher RF currents.

For PIN diodes, the maximum current rating should be specified or is dependent upon the diode power dissipation rating, while the maximum voltage stress at RF frequencies is dependent on I region thickness.

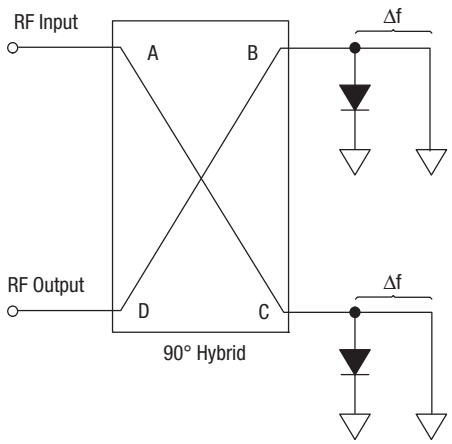


Figure 31. Hybrid Coupler Reflective Phase Shifter

PIN Diode Distortion Model

This Application Note has described large signal operation and thermal considerations that allow the circuit designer to avoid conditions that would lead to significant changes in PIN diode performance or excessive power dissipation. A subtle, but often significant, operating characteristic is the distortion or change in signal shape, which is always produced by a PIN diode in the signal it controls.

The primary cause of distortion is any variation or nonlinearity of the PIN diode impedance during the period of the applied RF signal. These variations could be in the diode's forward bias resistance, R_S, parallel resistance, R_P, capacitance, C_T, or the effect of the low frequency I-V characteristic.

The level of distortion can range from better than 100 dB below, to levels approaching the desired signal. The distortion could be analyzed in a Fourier series and takes the traditional form of harmonic distortion of all orders, when applied to a single input signal, and harmonic intermodulation distortion when applied to multiple input signals.

Nonlinear, distortion-generating behavior is often desired in PIN and other RF oriented semiconductor diodes. Self-biasing limiter diodes are often designed as thin I region PIN diodes operating near or below their transit time frequency. In a detector or mixer diode, the distortion that results from the ability of the diode to follow its I-V characteristic at high frequencies is exploited.

In this regard, the term "square law detector" applied to a detector diode implies a second order distortion generator. In the PIN switch circuits described at the beginning of this Application Note, and the attenuator and other applications described here, methods of selecting and operating PIN diodes to obtain low distortion have been described.

There is a common misconception that minority carrier lifetime is the only significant PIN diode parameter that affects distortion.

This is indeed a major factor but another important parameter is the width of the I region, which determines the transit time of the PIN diode. A diode with a long transit time has more of a tendency to retain its quiescent level of stored charge. The longer transit time of a thick PIN diode reflects its ability to follow the stored charge model for PIN diode resistance according to the following relationships.

$$Q = I_F \tau \tag{44}$$

Where the stored charge, *Q*, is in coulombs.

$$R_S = \frac{W^2}{(\mu p + \mu n)Q} \tag{45}$$

Where: I_F = forward bias current
τ = carrier lifetime
W = I region width
μn = electron mobility
μp = hole mobility
R_S = series resistance in Ω

The effect of carrier lifetime on distortion relates to the quiescent level of stored charge induced by the DC forward bias current and the ratio of this stored charge to the incremental stored charge added or removed by the RF signal.

The distortion generated by a forward biased PIN diode switch has been analyzed and has been shown to be related to the ratio of stored charge to diode resistance and the operating frequency.

The following prediction equations for the second order intermodulation intercept point (IP2) and the third order intermodulation intercept point (IP3) have been developed from PIN semiconductor analysis.

$$IP2 = 34 + 20\log\left(\frac{F \times Q}{R_S}\right) \tag{46}$$

$$IP2 = 34 + 20\log\left(\frac{F \times Q}{R_S}\right) \tag{47}$$

$$IP3 = 21 + 15\log\left(\frac{F \times Q}{R_S}\right) \tag{48}$$

Where: *IP2* = 2nd Order Insertion Point in dBm
IP3 = 3rd Order Insertion Point in dBm
F = frequency in MHz
R_S = PIN diode resistance in Ω
Q = stored charge in nC

In most applications, the distortion generated by a reversed biased diode is smaller than forward biased generated distortion for small or moderate signal size. This is particularly the case when the reverse bias applied to the PIN diode is larger than the peak RF voltage, which prevents any instantaneous swing into the forward bias direction.

Distortion produced in a PIN diode circuit may be reduced by connecting an additional diode in a back-to-back orientation (cathode-to-cathode or anode-to-anode). This results in a cancellation of distortion currents. The cancellation should be total, but the distortion produced by each PIN diode is not exactly equal in magnitude and opposite in phase. Approximately 20 dB distortion improvement may be expected by this back-to-back configuration.

Distortion in Attenuator Circuits

In attenuator applications, distortion is directly relatable to the ratio of RF to DC stored charge. In such applications, PIN diodes operate only in the forward bias state, and often at high resistance values where the stored charge may be very low. Under these operating conditions, distortion varies with charges in the attenuation level. Therefore, PIN diodes selected for use in attenuator circuits need be chosen only for their thick I region width, since the stored charge at any fixed diode resistance, R_S, is dependent only on this dimension.

Consider the Skyworks SMP1304-001 PIN diode used in an application where a resistance of 50 Ω is desired. The Data Sheet (document #200044) indicates that 1 mA is the typical diode current at which this occurs. Since the typical carrier lifetime for this diode is 1 μs, the stored charge for the diode at 50 Ω is 1.0 nC.

However, if two PIN diodes are inserted in series to achieve the same 50 Ω resistance level, each diode must be biased at 2 mA. This results in a stored charge of 2 nC per diode, or a net stored charge of 4 nC. Therefore, adding a second diode in series multiplies the effective stored charge by a factor of 4. This would have a significant positive impact on reducing the distortion produced by attenuator circuits.

Measuring Distortion

Because distortion levels are often 50 dB or more below the desired signal, special precautions are required to make accurate second and third order distortion measurements.

One must first ensure that the signal sources used are free of distortion and that the dynamic range of the spectrum analyzer used is adequate to measure the specified level of distortion. These requirements often lead to the use of fundamental frequency bandstop filters at the device output, as well as preselectors to clean up the signal sources used.

To establish the adequacy of the test equipment and signal sources for making the desired distortion measurements, the test circuit should be initially evaluated by removing the diodes and replacing them with passive elements. This approach permits one to optimize the test setup and establish basic measurement limitations.

Since harmonic distortion appears only at multiples of the signal frequency, these signals may be filtered out in narrow band systems. Second order distortion, caused by the mixing of two input signals, appears at the sum and difference of these frequencies and may also be filtered.

To help identify the various distortion signals seen on a spectrum analyzer, it should be noted that the level of a second distortion signal will vary directly at the same rate as any change of input signal level. Therefore, a 10 dB signal increase causes a corresponding 10 dB increase in second order distortion.

Third order intermodulation distortion of two input signals at frequencies F_A and F_B often produce in-band, nonfilterable distortion components at frequencies of $2F_A - F_B$ and $2F_B - F_A$.

This type of distortion is particularly troublesome in receivers located near transmitters that operate on equally spaced channels. When such signals are identified and measured, it should be noted that third order distortion signal levels vary at twice the rate of change of the fundamental signal frequency. Therefore, a 10 dB change in input signal results in a 20 dB change of the third order signal distortion power observed on a spectrum analyzer.

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