

DATA SHEET

SKY66312-11: 2300 to 2400 MHz Wide Instantaneous Bandwidth High-Efficiency Power Amplifier

Applications

- 4G LTE and 5G NR systems
- Supports 3GPP Bands 30 and 40
- Driver amplifier for micro base stations and macro base stations
- Enterprise small-cell and massive MIMO

Features

- Wide instantaneous signal bandwidth: 100 MHz
- High-efficiency: PAE = 36% @ +28dBm
- High linearity: +28 dBm with < -50 dBc ACLR with pre-distortion (100 MHz LTE, 8.5 dB PAR signal)
- High gain: 35 dB
- Excellent input and output return loss: to 50 Ω system
- Integrated active bias: performance compensated over temp
- Integrated enable On/Off function: PAEN_{HIGH} = 1.7 to 2.5 V
- Single supply voltage: 5.0 V
- Pin-to-pin compatible PA family supporting major 3GPP bands
- Compact (16-pin, 5 × 5 × 1.3 mm) package (MSL3, 260 °C per JEDEC J-STD-020)



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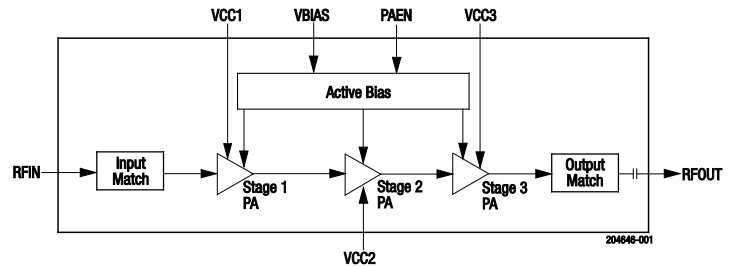


Figure 1. SKY66312-11 Block Diagram

Description

The SKY66312-11 is a highly efficient, wide instantaneous bandwidth, fully input/output matched power amplifier (PA) with high gain and linearity. The compact 5 × 5 mm PA is designed for 4G LTE and 5G NR systems operating from 2300 to 2400 MHz. The active biasing circuitry is integrated to compensate PA performance over temperature, voltage, and process variation.

The SKY66312-11 is part of a high-efficiency, pin-to-pin compatible PA family supporting major 3GPP bands.

A block diagram of the SKY66312-11 is shown in Figure 1. The device package and pinout for the 16-pin device are shown in Figure 2. Table 1 lists the top 5G parts in the pin-to-pin compatible PA family. Signal pin assignments and functional pin descriptions are described in Table 2.

Table 1. Pin-to-Pin Compatible PA Family

Part Number	Frequency (MHz)	3GPP Band/5G Band
SKY66312-11	2300 to 2400	Bands 30 and 40
SKY66317-11	2496 to 2690	Bands 7, 38, and 41
SKY66318-11	3300 to 3600	n78
SKY66318-21	3300 to 3700	n78
SKY66319-11	4400 to 5000	n79

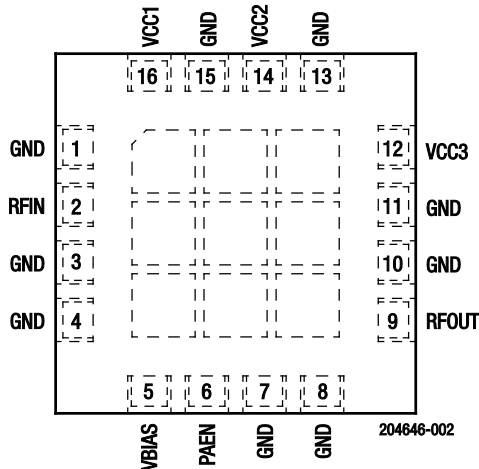


Figure 2. SKY66312-11 Pinout (Top View)

Table 2. SKY66312-11 Signal Descriptions¹

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	9	RFOUT	RF output port
2	RFIN	RF input port	10	GND	Ground
3	GND	Ground	11	GND	Ground
4	GND	Ground	12	VCC3	Stage 3 collector voltage
5	VBIAS	Bias voltage	13	GND	Ground
6	PAEN	PA enable	14	VCC2	Stage 2 collector voltage
7	GND	Ground	15	GND	Ground
8	GND	Ground	16	VCC1	Stage 1 collector voltage

¹ The center ground pad must have a low inductance and low thermal resistance connection to the application's printed circuit board ground plane.

Technical Description

The matching circuits are contained within the device. An on-chip active bias circuit is included within the device for both input and output stages, which provides excellent gain tracking over temperature and voltage variations.

The SKY66312-11 is internally matched for maximum output power and efficiency. The input and output stages are independently supplied using the VCC1, VCC2, and VCC3 supply lines (pins 16, 14, and 12, respectively). The DC control voltage that sets the bias is supplied by the Vbias signal (pin 5).

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY66312-11 are provided in Table 3. Recommended operating conditions are specified in Table 4, and electrical specifications are provided in Table 5.

Typical performance characteristics are shown in Figures 3 through 20.

Table 3. SKY66312-11 Absolute Maximum Ratings¹

Parameter	Symbol	Minimum	Maximum	Units
RF input power (CW, 50 Ω load)	P _{IN}		+8	dBm
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V _{CC}		5.5	V
PA enable	V _{EN}		2.8	V
Operating temperature	T _C	-40	+115	°C
Storage temperature	T _{ST}	-55	+125	°C
Junction temperature	T _J		+150	°C
Power dissipation	P _D		1.2	W
Device thermal resistance	θ _{JC}		15	°C/W

¹ Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD HANDLING: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 4. SKY66312-11 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V _{CC1} , V _{CC2} , V _{CC3} , V _{BIAS}	4.75	5	5.25	V
PA enable:	PAEN				
ON		1.7	2.0	2.5	V
OFF			0	0.5	V
PA enable current	I _{ENABLE}		1	12	μA
Operating frequency	f	2300		2400	MHz
Operating temperature	T _C	-40	+25	+115	°C

Table 5. SKY66312-11 Electrical Specifications¹

(Vcc1 = Vcc2 = Vcc3 = VBIAS = 5 V, PAEN = 2.0 V, f = 2350 MHz, Tc = +25 °C, Input / Output Load = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	f		2300		2400	MHz
Small signal gain	IS21I	PIN = -30 dBm	34	35		dB
Gain @ +23 dBm	IS21I@+23 dBm	POUT = +23 dBm	34	35		dB
Gain @ +28 dBm	IS21I@+28 dBm	POUT = +28 dBm		35		dB
Input return loss	IS11I	PIN = -20 dBm	11	12		dB
Output return loss	IS22I	PIN = -20 dBm	10	15		dB
Reverse isolation ²	IS12I	PIN = -30 dBm		50		dB
ACLR @ +23 dBm	ACLR	POUT = +23 dBm (5x20 MHz LTE, 8.5 dB PAR signal)		-30.5	-27	dBc
ACLR @ +28 dBm ²	IS21I@+28 dBm	POUT = +28 dBm (5x20 MHz LTE, 8.5 dB PAR signal)		-26		dBc
Output power at 1dB gain compression ²	P1dB	CW, reference to small signal gain (PIN = -30 dBm)	+31	+32		dBm
Output power at 3dB gain compression	P3dB	CW, reference to small signal gain (PIN = -30 dBm)	+35.3	+36.5		dBm
2 nd harmonic	2fo	CW, POUT = +23 dBm		-43	-35	dBc
3 rd harmonic	3fo	CW, POUT = +23 dBm		-55	-45	dBc
Power-added efficiency	PAE	CW, POUT = +23 dBm	18.5	20		%
Quiescent current	ICQ	No RF signal		75	100	mA
Load mismatch stress with no permanent degradation or failure ²		VCC = +5 V, POUT = +23 dBm @ 50 Ω with 20 MHz LTE signal, PAR = 8.5 dB		6:1		VSWR
RF turn-on time ³	tON			1.7	3	us

¹ Performance is guaranteed only under the conditions listed in this table.

² Not tested in production. Verified by characterization.

³ RF turn-on time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power achieves 90% of the average steady-state "on" level.

Typical Performance Characteristics

(VCC1 = VCC2 = VCC3 = VBIAS = 5 V, PAEN = 2.0 V, f = 2350 MHz, Tc = 25 °C, Input / Output Load = 50 Ω, Unless Otherwise Noted)

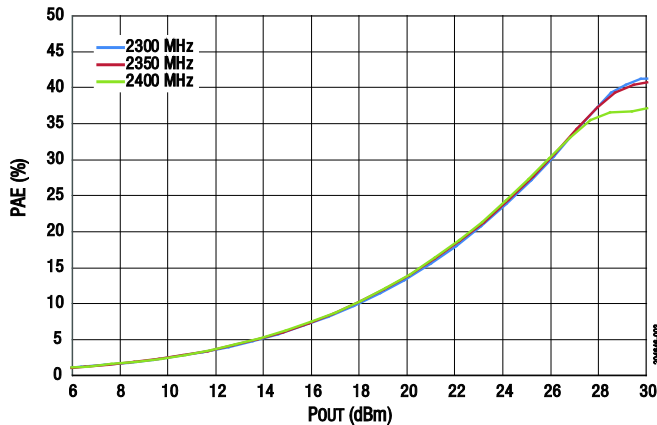


Figure 3. PAE vs POUT Across Frequency

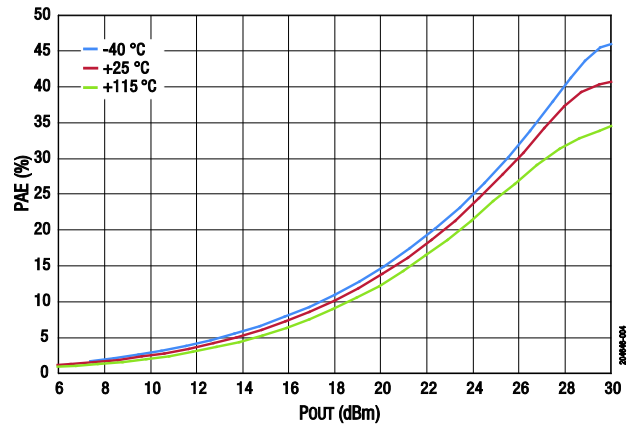


Figure 4. PAE vs POUT Across Temperature

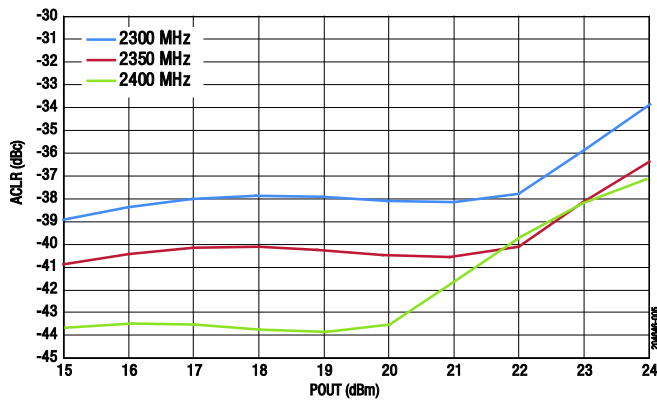


Figure 5. ACLR (1x20 MHz) vs POUT Across Frequency

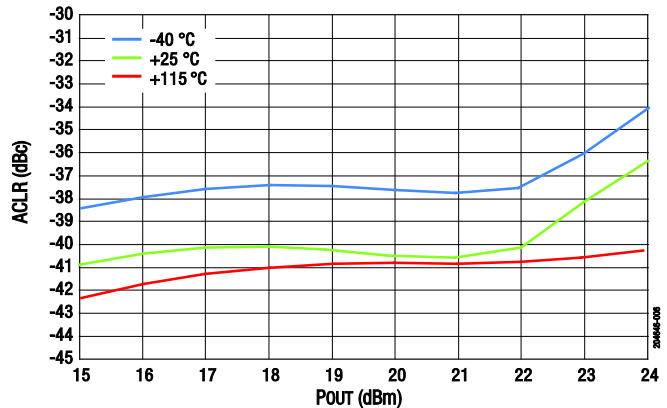


Figure 6. ACLR (1x20 MHz) vs POUT Across Temperature

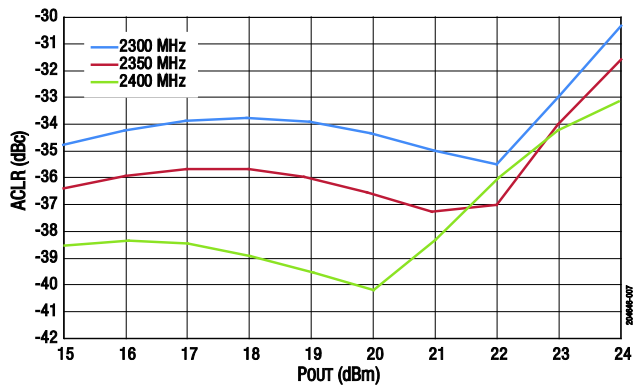


Figure 7. ACLR (3x20 MHz) vs POUT Across Frequency

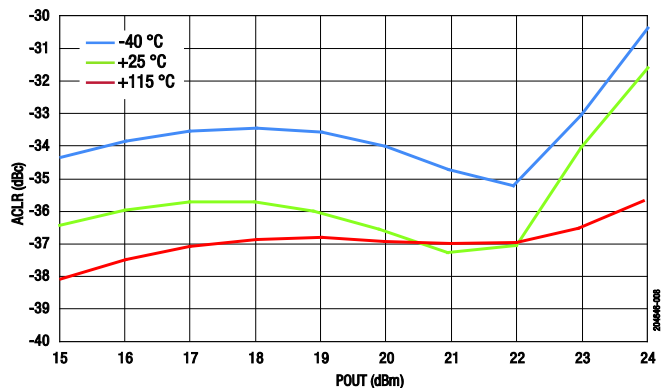


Figure 8. ACLR (3x20 MHz) vs POUT Across Temperature

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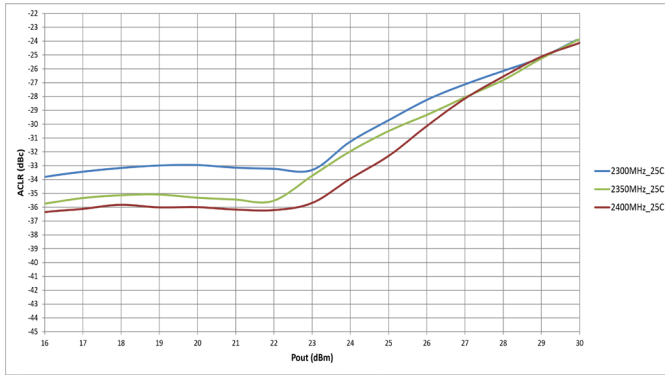


Figure 9. ACLR vs POUT over Frequency (5x20 MHz)

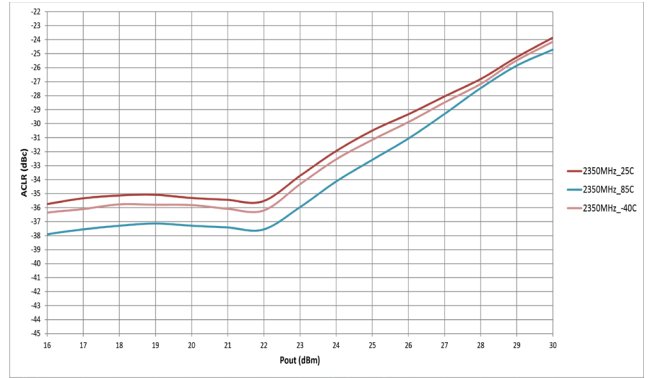


Figure 10. ACLR vs POUT over Temperature (5x20 MHz)

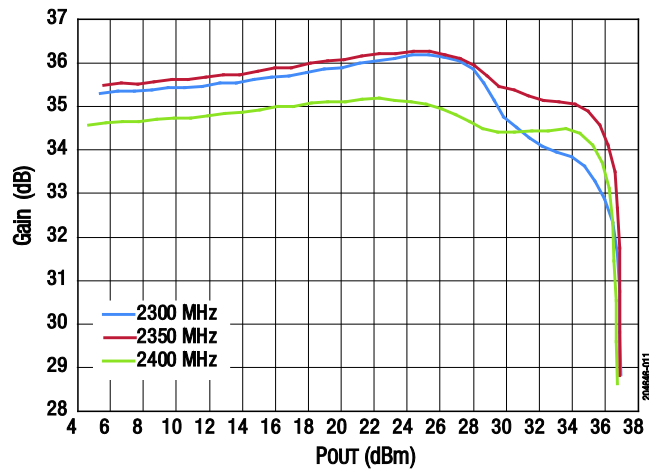


Figure 11. Gain vs POUT Across Frequency

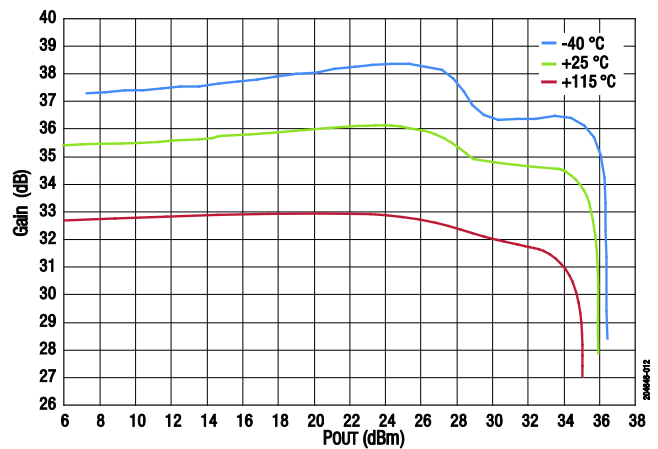


Figure 12. Gain vs POUT Across Temperature

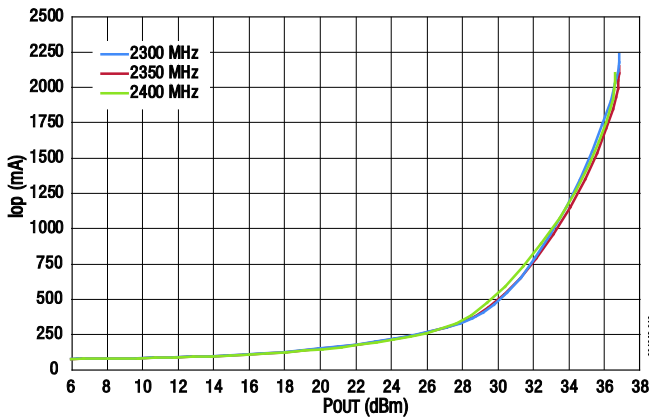


Figure 13. Operating Current vs POUT Across Frequency

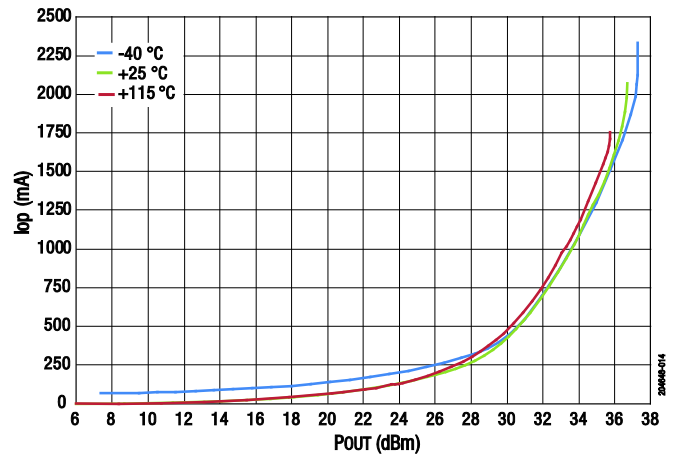


Figure 14. Operating Current vs POUT Across Temperature

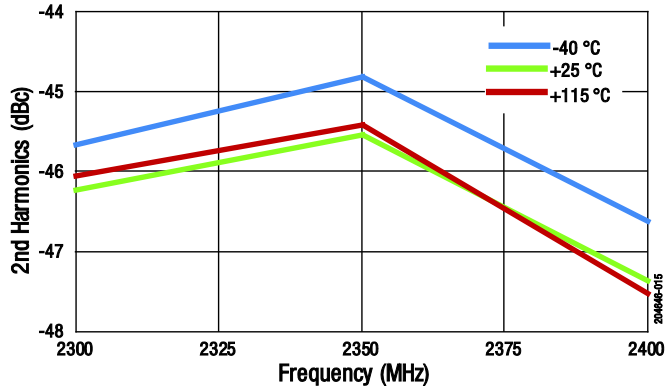


Figure 15. 2nd Harmonic vs Frequency Across Temperature @ POUT = +23 dBm (CW)

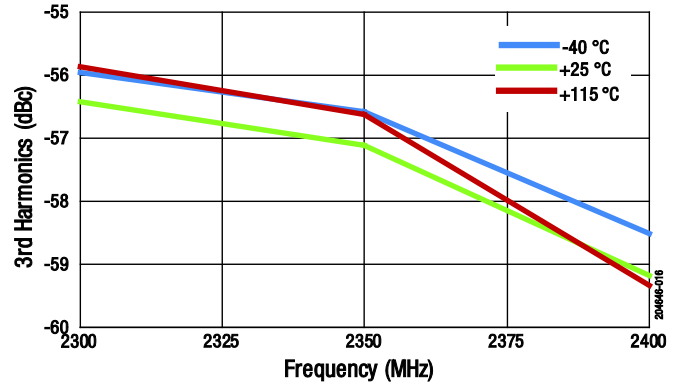


Figure 16. 3rd Harmonic vs Frequency Across Temperature @ POUT = +23 dBm (CW)

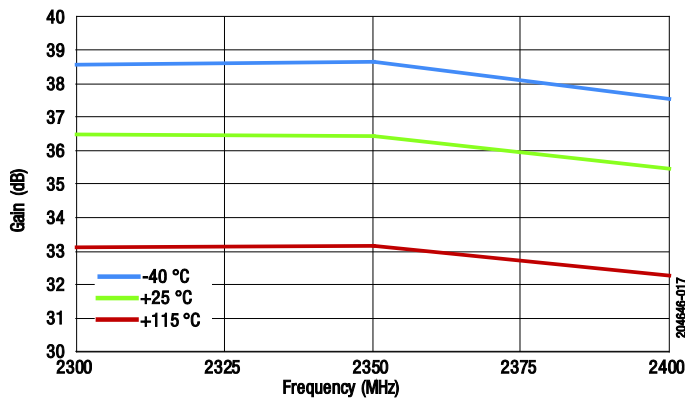


Figure 17. Small Signal Gain vs Frequency Across Temperature (PIN = -20 dBm)

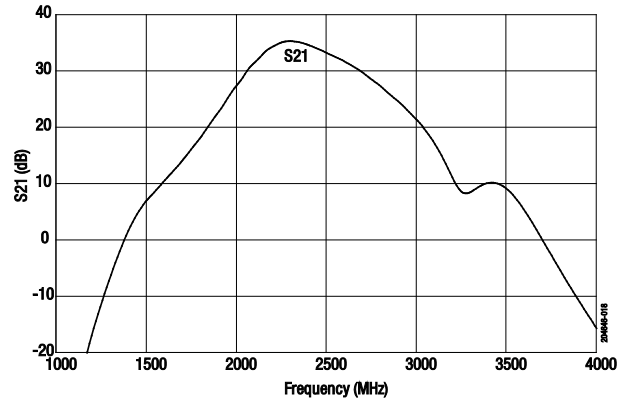


Figure 18. S21 vs Frequency

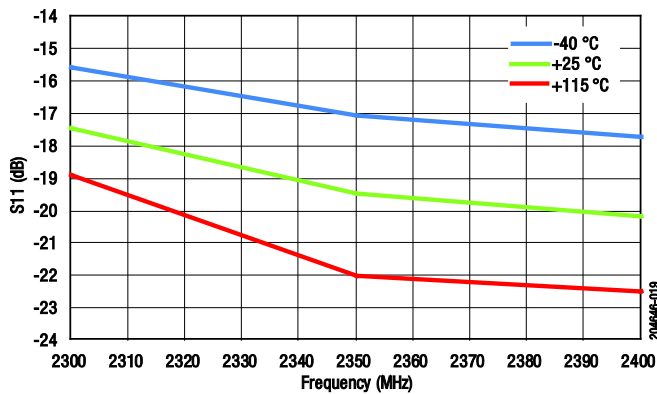


Figure 19. Input Return Loss vs Frequency Across Temperature (Small Signal, PIN = -20 dBm)

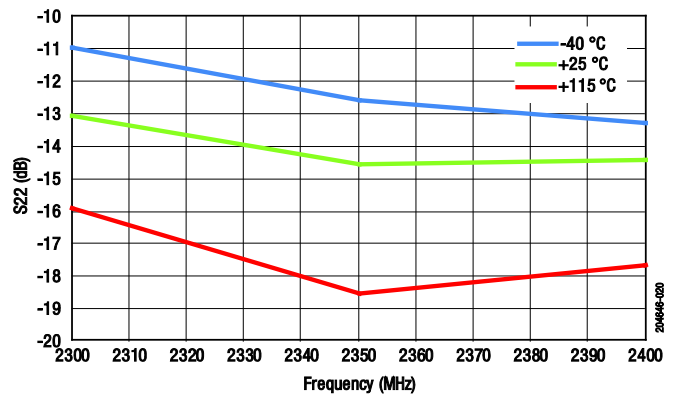


Figure 20. Output Return Loss vs Frequency Across Temperature (Small Signal, PIN = -20 dBm)

Evaluation Board Description

The SKY66312-11 Evaluation Board is used to test the performance of the SKY66312-11 PA. An application schematic is provided in Figure 21. Table 6 provides the Bill of Materials (BOM) list for Evaluation Board components.

An assembly drawing for the Evaluation Board is shown in Figure 18. Board layer details are shown in Figure 22. Layer detail physical characteristics are noted in Figure 23.

Evaluation Board Test Procedure

Turn-On Sequence

1. Connect 50 Ω Test Equipment or Load to the input and output RF ports of the Evaluation Board.
2. Connect the DC ground.
3. Connect all VCCs and VBIAS lines to a +5 V supply. Connect PAEN to a 2.0 V supply.
4. Without applying RF, turn on the 5 V supply, then turn on the 2 V PAEN.
5. Apply RF signal data at -30 dBm and observe that the gain of the device is approximately 35 dB. Begin measurements.

Turn-Off Sequence

1. Turn off the RF input to the device.
2. Turn off PAEN (set to 0 V).
3. Turn off all VCCs and VBIAS.

NOTE: It is important to adjust the VCC voltage sources so that +5 V is measured at the board. High collector currents drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

- Paths to ground should be made as short as possible.
- The ground pad of the SKY66312-11 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Because the circuit board acts as the heat sink, it must shunt as much heat as possible from the device.

Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

NOTE: A poor connection between the ground pad and ground increases junction temperature (T_J), which reduces the life of the device.

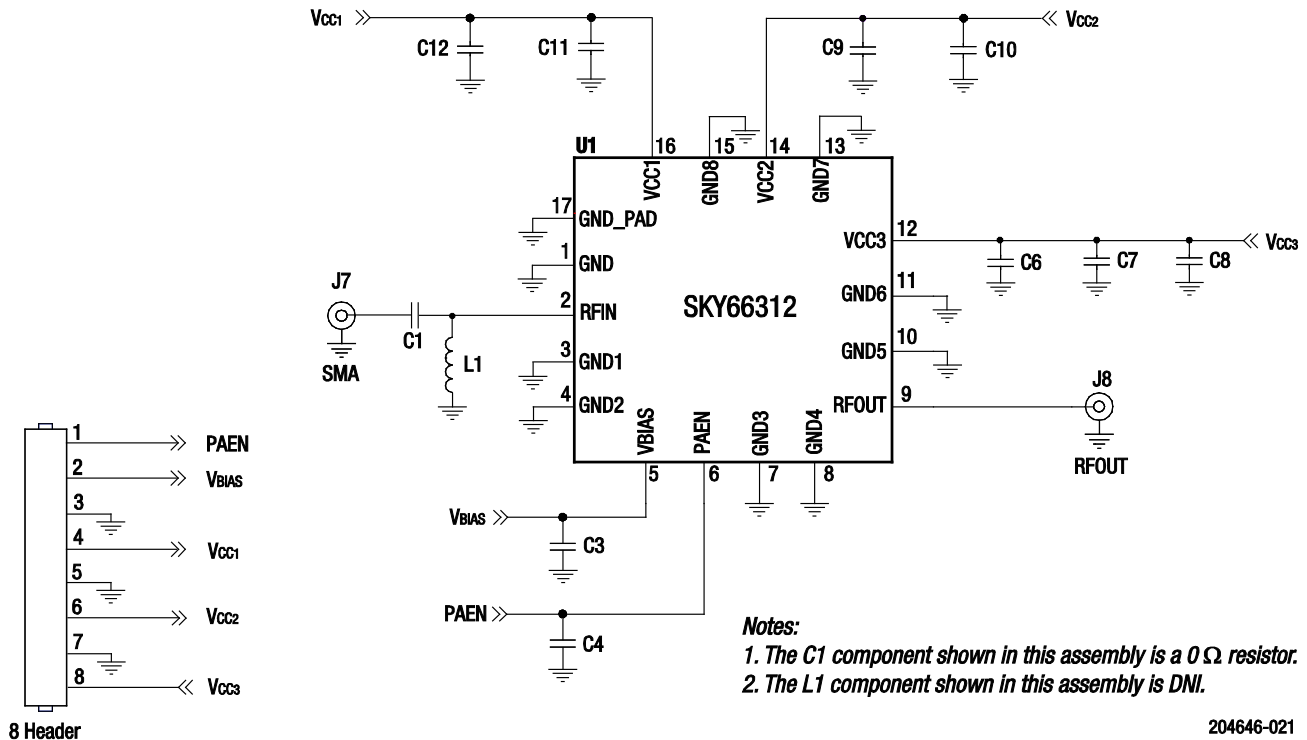
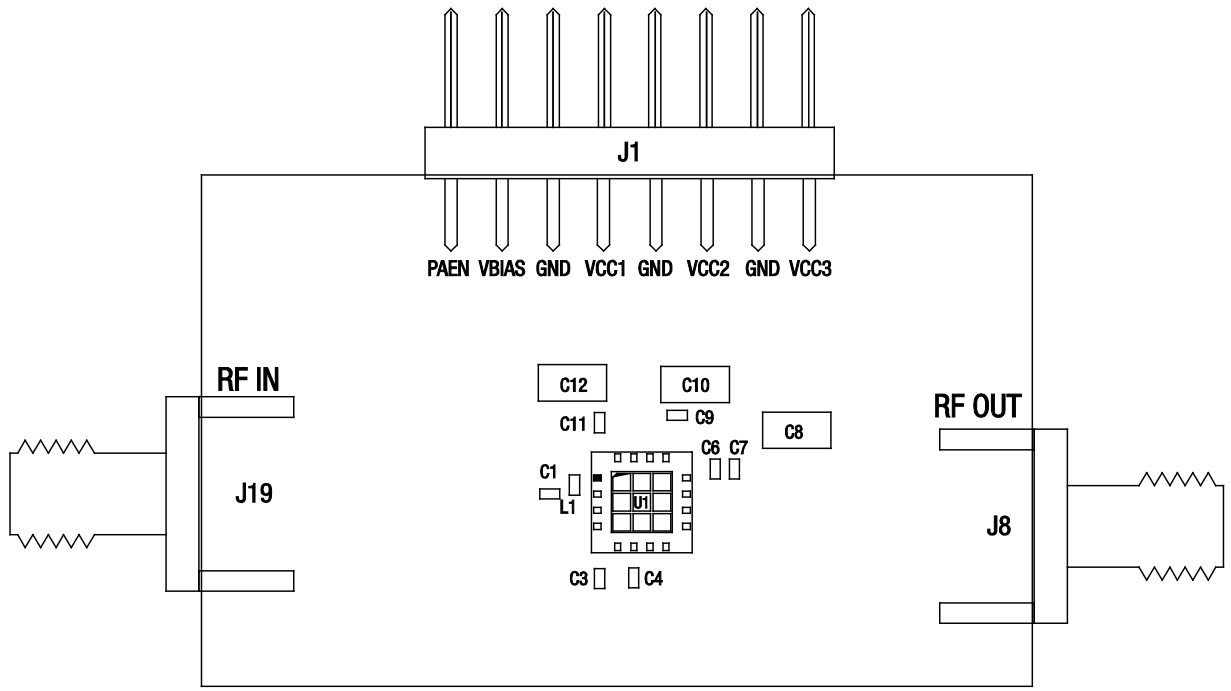


Figure 21. SKY66312-11 Application Schematic

Table 6. SKY66312-11 Evaluation Board Bill of Materials (BOM)

Component	Description	Size
C1	Resistor, 0 Ω, 0.063 W	0402
C3	Ceramic capacitor, 1 μF, ±10%, 16 V	0402
C4, C7	Ceramic capacitor, 3300 pF, X7R, ±10%, 50 V	0402
C6, C9, C11	Ceramic capacitor, 0.47 μF	0402
C8, C10, C12	Ceramic capacitor, 10 μF, X7R, ±10%, 16 V	1206
L1	DNI	
TW21-D695-013	Evaluation Board	



- Notes:**
1. Evaluation Board Gerber files are available on request.
 2. The C1 component shown in this assembly is a 0Ω resistor.
 3. The L1 component shown in this assembly is DNI.

Figure 22. Evaluation Board Assembly Drawing

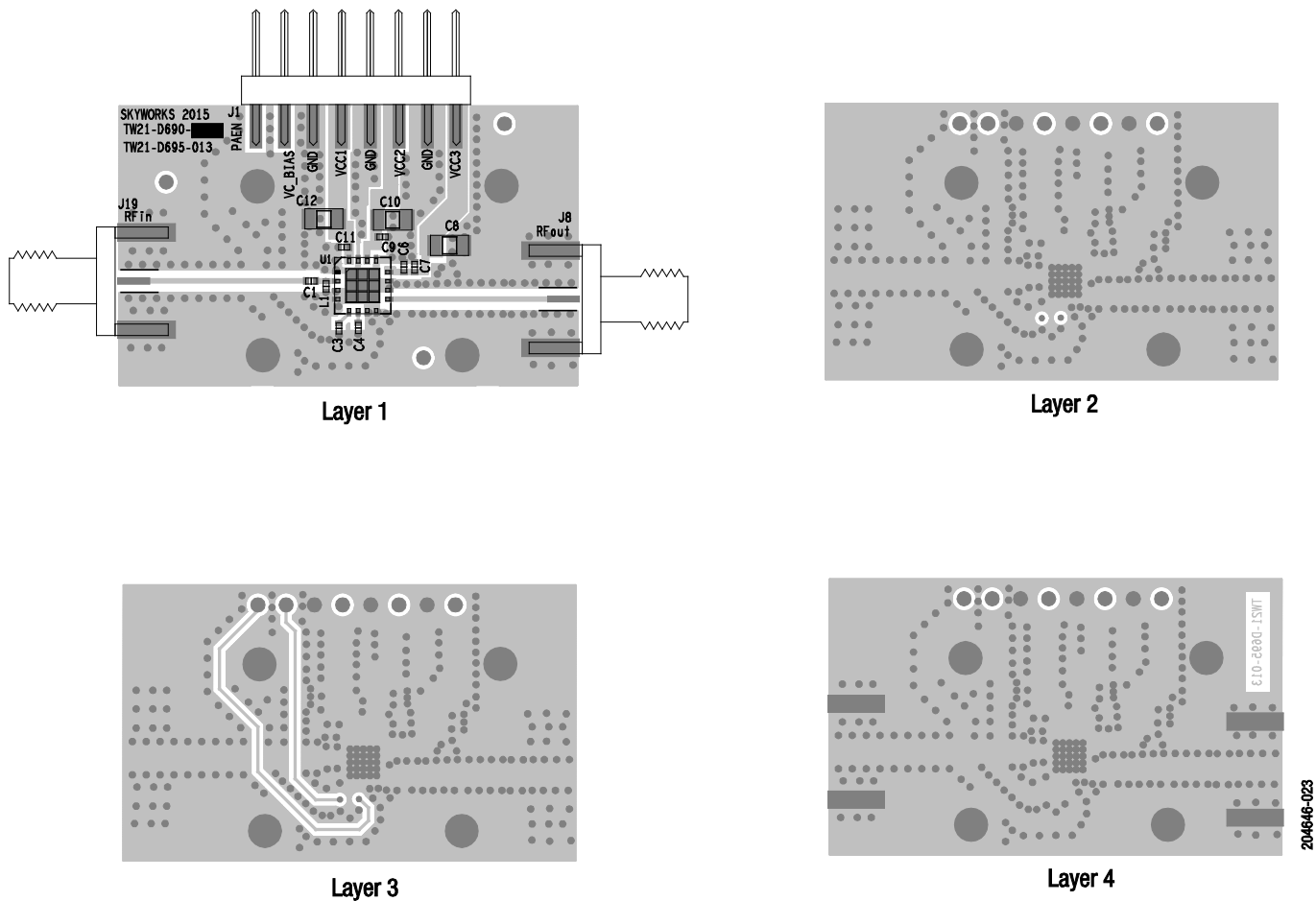


Figure 23. Board Layer Detail

50 Ohm	Cross Section	Name	Thickness (mm)	Materials
W = 0.500 mm 		TMask	0.010	Solder Resist
		L1	0.035	Cu, 1 oz.
		Dielectric	0.250	R04350
		L2	0.035	Cu, 1 oz.
		Dielectric	0.350	FR4
		L3	0.035	Cu, 1 oz.
		Dielectric	0.250	FR4
		L4	0.035	Cu, 1 oz.
		BMask	0.010	Solder Resist

204646-024

Figure 24. Layer Detail Physical Characteristics

Application Circuit Notes

Center Ground. It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and work well under the device if solder migration is an issue.

GND (pins 1, 3, 4, 7, 8, 10, 11, 13, and 15). Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

VCBIAS (pin 5). The bias supply voltage for each stage, nominally set to +5 V.

RFOUT (pin 9). Amplifier RF output pin ($Z_0 = 50 \Omega$). The module includes an internal DC blocking capacitor. All impedance matching is provided internal to the module.

VCC1, VCC2, and VCC3 (pin 16, 15, and 12, respectively). Supply voltage for each stage collector bias is nominally set to 5 V. The evaluation board has inductors L1 and L2. These are place holders and should be populated with 0Ω resistors. Bypass and decoupling capacitors C6 through C12 should be placed in the approximate location shown on the evaluation board assembly drawing, although exact placement is not critical.

RFIN (pin 2). Amplifier RF input pin ($Z_0 = 50 \Omega$). All impedance matching is provided internal to the module.

Package Dimensions

Typical part marking for the device is shown in Figure 25. The PCB layout footprint for the SKY66312-11 is shown in Figure 26. Package dimensions are shown in Figure 27, and tape and reel dimensions are provided in Figure 28.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY66312-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

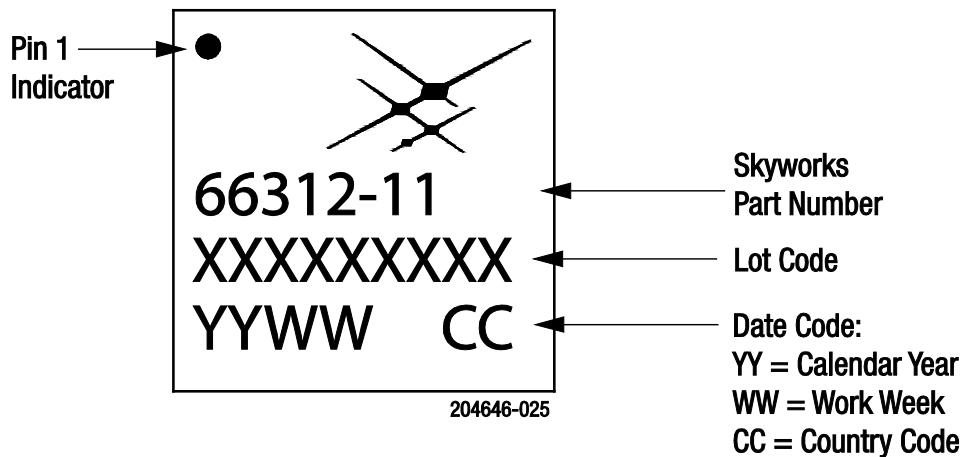


Figure 25. SKY66312-11 Typical Part Marking

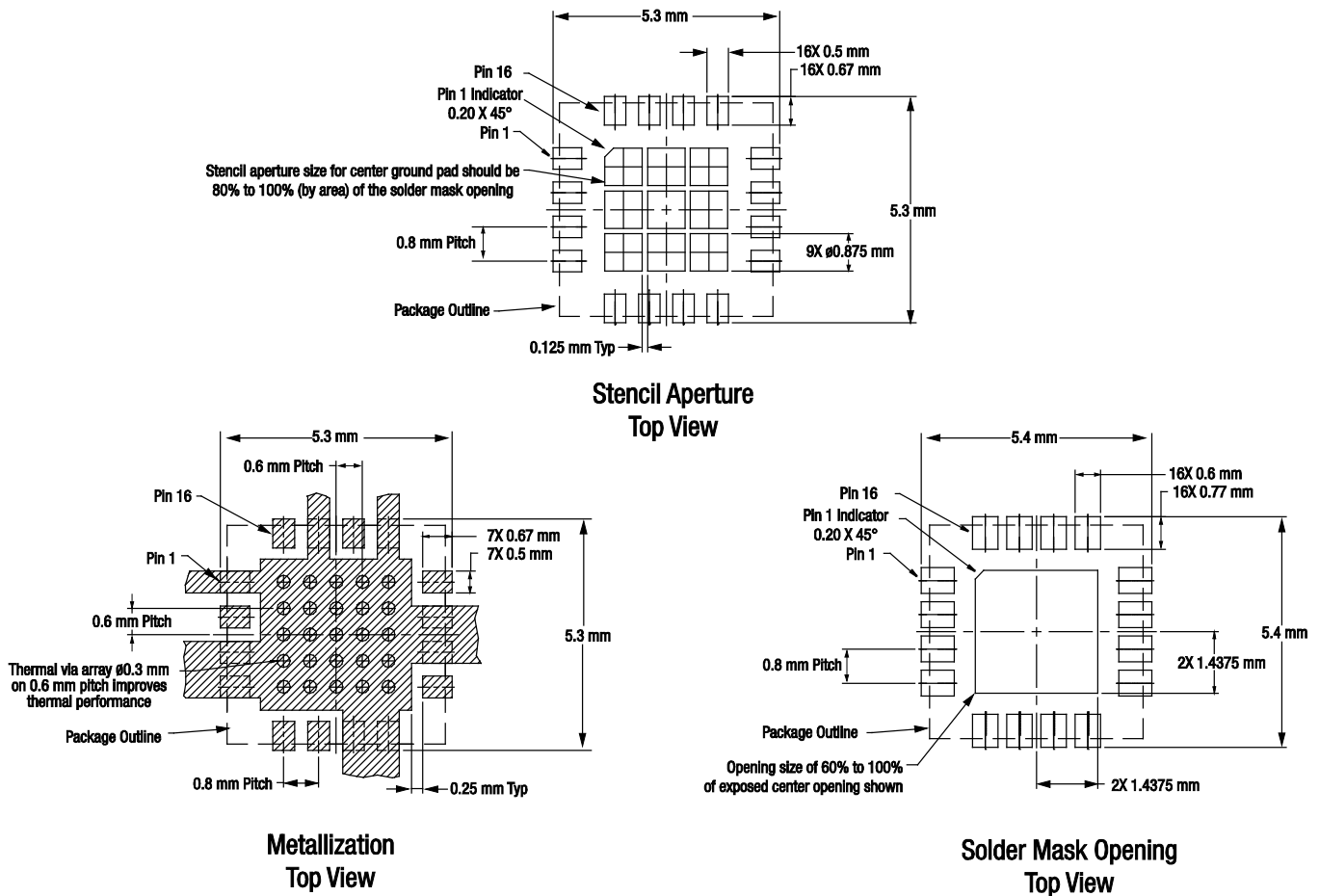
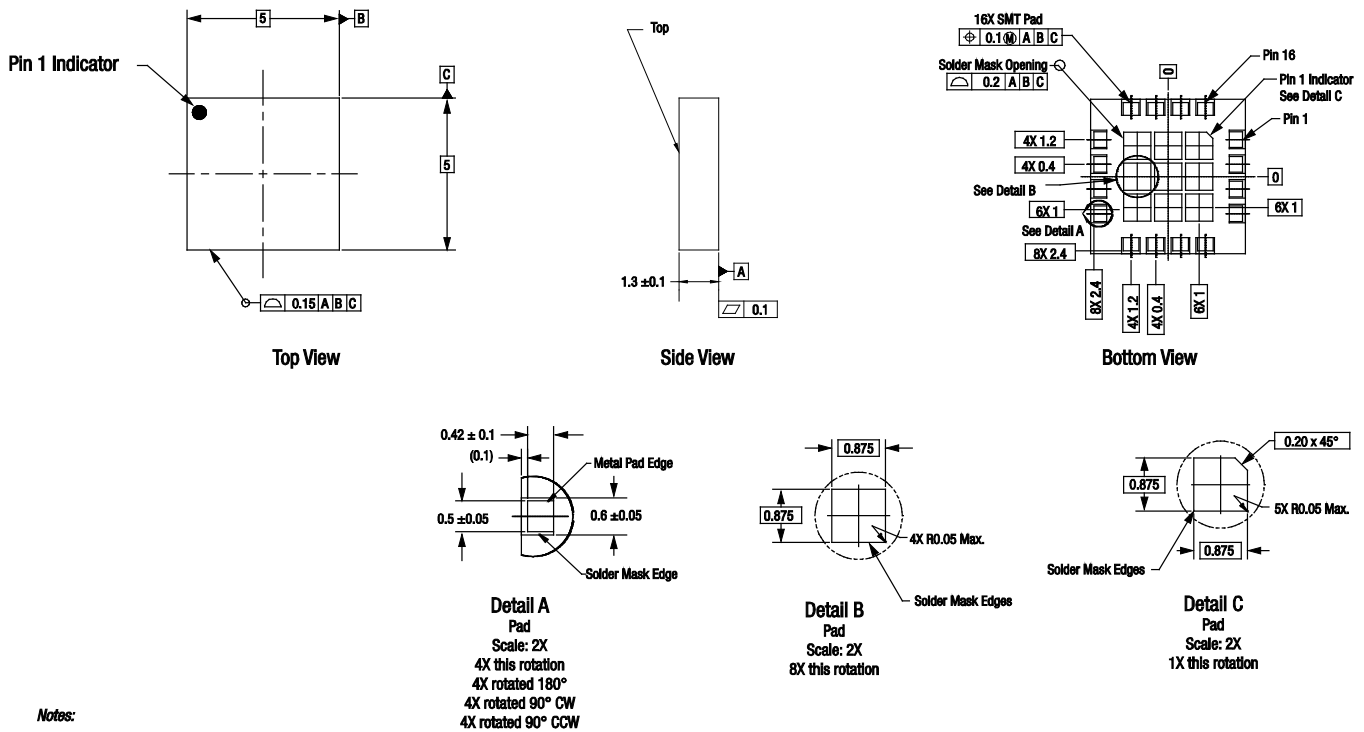


Figure 26. SKY66312-11 PCB Layout Footprint

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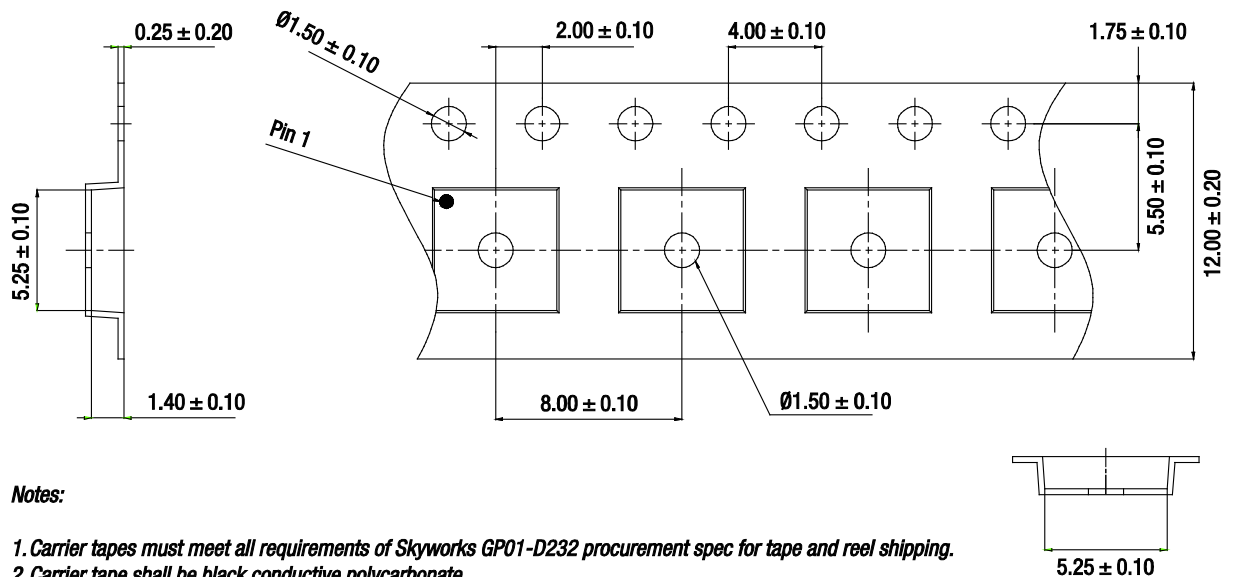


Notes:

1. Dimensions are in millimeters (unless otherwise specified).
2. Dimensions and tolerances are in accordance with ASME Y14.5M-1994.

204646-027

Figure 27. SKY66312-11 Package Dimensions



204646-028

Figure 28. SKY66312-11 Tape and Reel Dimensions

Ordering Information

Product Description	Product Part Number	Evaluation Board Part Number
SKY66312-11: 2300 to 2400 MHz Wide Instantaneous High-Efficiency PA	SKY66312-11	SKY66312-11EK1

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