Cascading Two Si53112 Buffers

1. Introduction

It is becoming more common in server and storage applications to require more than twenty 100 MHz PCIe Gen2/3 clock outputs for various system functions and ICs. The highest output count PCIe Gen2/3 buffer available in the market provides 19 outputs, requiring board designers to cascade multiple buffers to achieve a higher number of outputs.

This application note provides schematic and design guidelines for cascading multiple Si53112 devices together, ensuring optimal input to output delay and PCIe gen jitter performance.

2. Board Design and Verification

Two concerns in cascaded PCIe clock buffer topologies are:

1. Propagation delay (from input of first buffer to outputs from the second buffer), and
2. PCIe Gen1/2/3 jitter performance.

To ensure the output clocks are within PCIe specifications in cascaded buffer topology, we have developed an evaluation board that cascades two Si53112 devices, with Si5338 being the frequency source. This board is shown in Figure 1.

The board features two types of traces:

1. Traces on the top layer in a 6-layer PCB.
2. Traces in the middle layer (layer-3) in a 6-layer PCB.

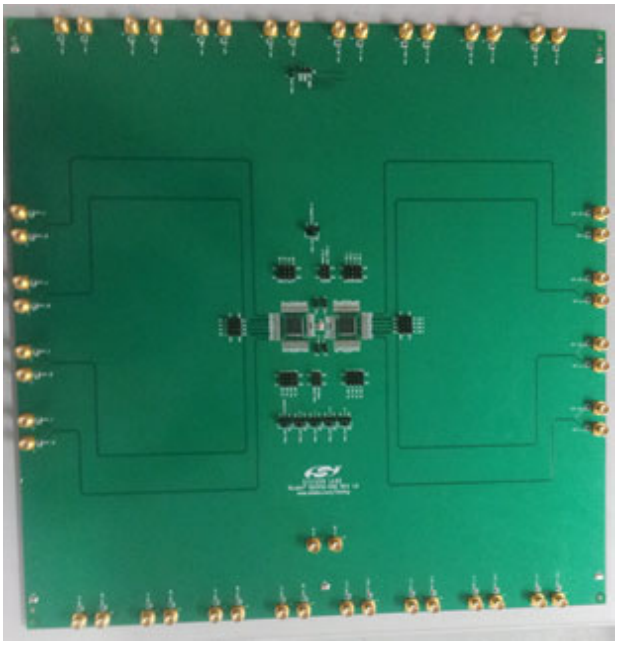

Figure 1. PCB with Two Cascaded Si53112 Devices

The board has the following design highlights:

1. Clock traces are 10 inches long for each output pair.
2. Each device has a dedicated power supply filter.
3. CLK0 output of the first device is the reference input to the second device.
4. Each device has dedicated control pins such as OE pins, BW/Bypass selection pin, etc.

The Skyworks Solutions PCIe buffers listed in Table 1 can operate in either fanout buffer or zero-delay buffer modes, and adhere to the performance specifications outlined in the DB800ZL, DB1200ZL, or DB1900Z PCIe requirements for server and storage motherboard design reference platforms.

Table 1. Skyworks Solutions PCIe Server Buffer Family

Part Number	Outputs	Output Buffer Type
Si53106	6	Push-Pull
Si53108	8	Push-Pull
Si53112	12	Push-Pull
Si53115	15	Push-Pull
Si53119	19	Push-Pull
Si53019	19	Constant Current

It should be noted that the analysis discussed in this application note is based on data taken on two cascaded Si53112 PCIe buffers; however, similar performance can be expected when cascading any two buffers noted in Table 1.

Our cascaded Si53112 test board was tested in zero-delay buffer mode (high loop band-width and low loop band-width modes), as well as fanout buffer mode. The subsequent sections present the measurement results of clock outputs in these three settings.

2.1. Signal Integrity Measurements

Table 2 shows the propagation delay (input to output skew) for various settings and Figures 2-10 show the oscilloscope shots.

Table 2. Input to Output Skew Measurements

Mode (both devices)	Skew (Input to Output of First Si53112)	Skew (Input of First to Output of Second Si53112)
Bypass mode	3.436 nS	7.108 nS
PLL mode, High Loop BW	–188.797 pS	–178.491 pS
PLL mode, Low Loop BW	–188.442 pS	–174.142 pS

Figure 2. Input Clock vs. Output Clock of 1st Si53112, Bypass Mode

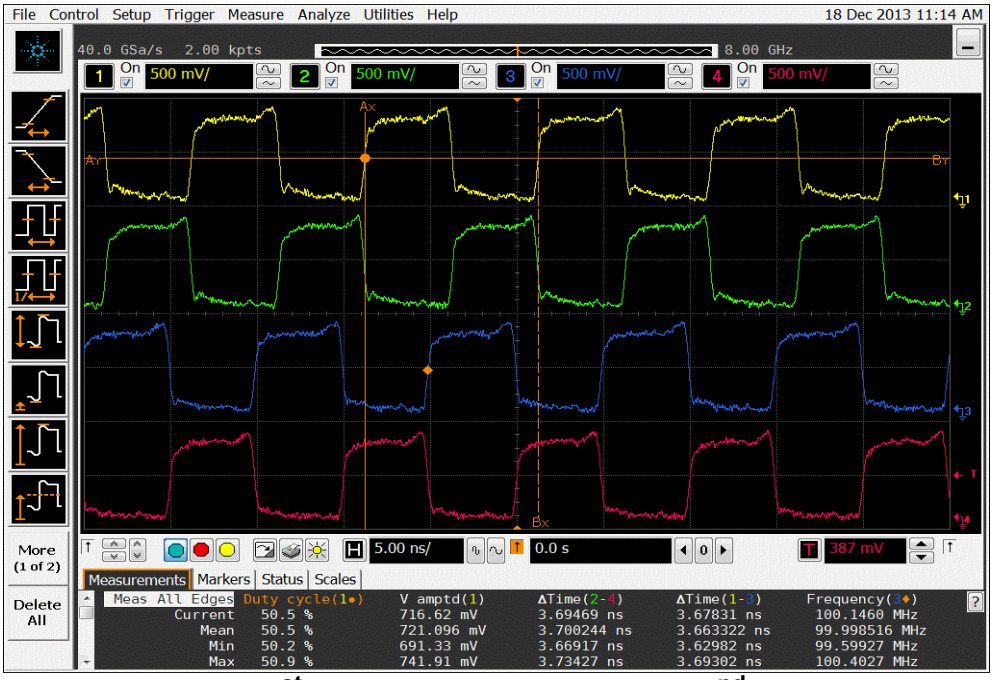

Figure 3. Output Clock of 1st Si53112 vs. Output Clock of 2nd Si53112, Bypass Mode

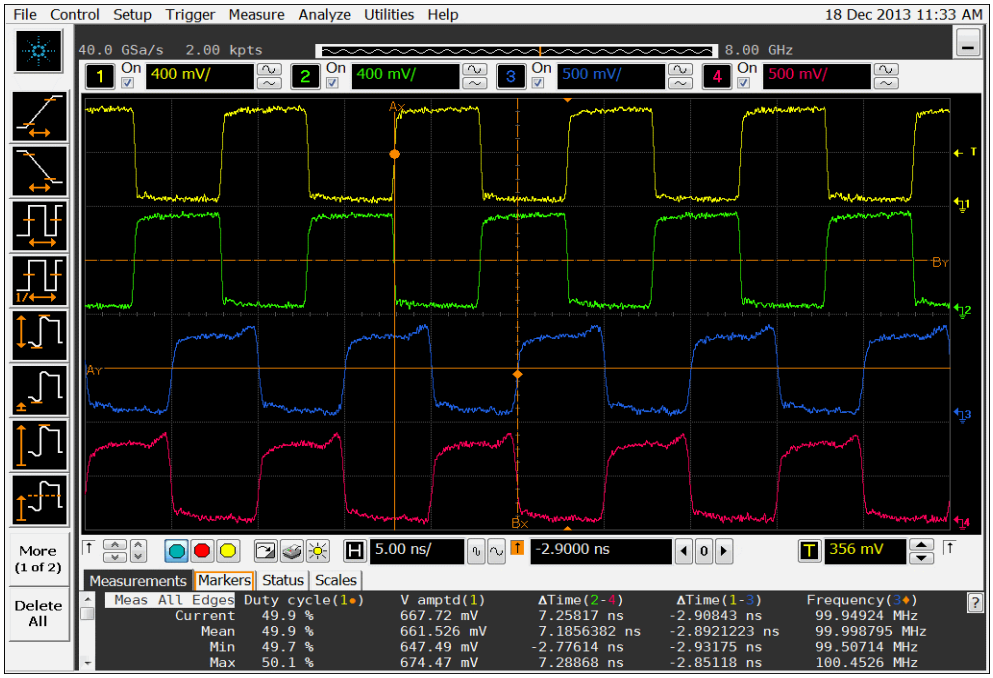

Figure 4. Input Clock vs. Output Clock of 2nd Si53112, Bypass Mode

Figure 5. Input Clock vs. Output Clock of 1st Si53112, HBW PLL Mode

Figure 6. Output Clock of 1st Si53112 vs. Output Clock of 2nd Si53112, HBW PLL Mode

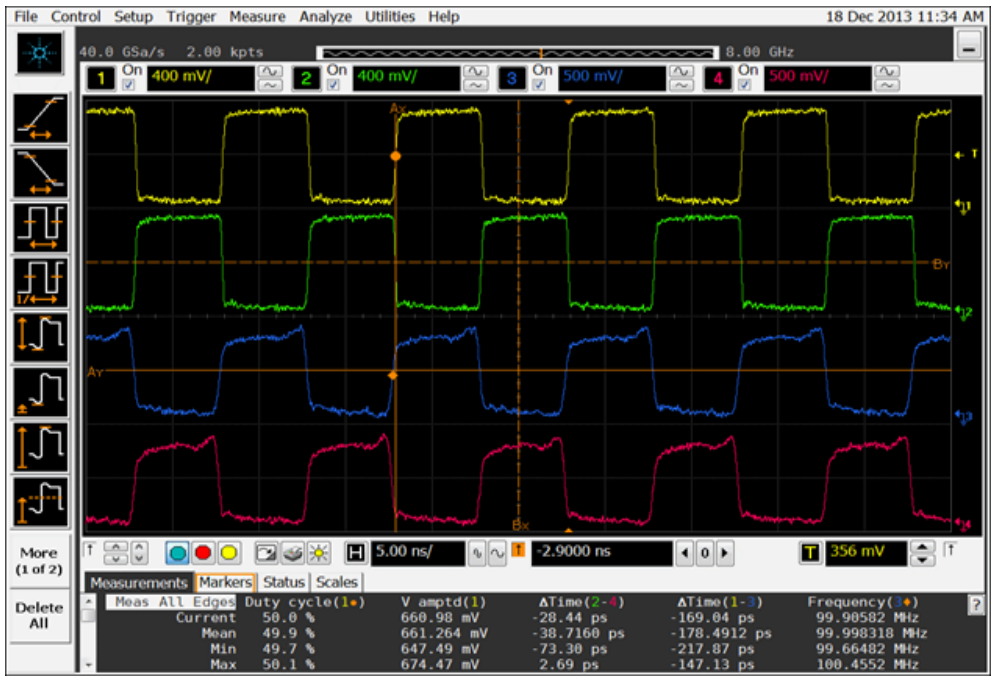

Figure 7. Input Clock vs. Output Clock of 2nd Si53112, HBW PLL Mode

Figure 8. Input Clock vs. Output Clock of 1st Si53112, LBW PLL Mode

Figure 9. Output Clock of 1st Si53112 vs. Output Clock of 2nd Si53112, LBW PLL Mode

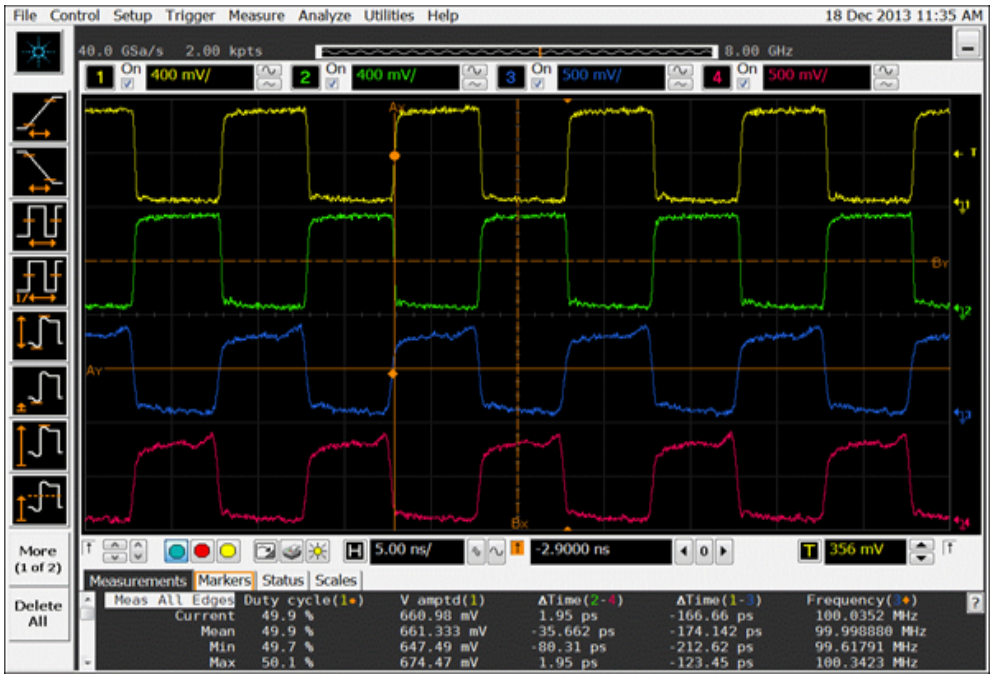

Figure 10. Input Clock vs. Output Clock of 2nd Si53112, LBW PLL Mode

2.2. PCIe Gen Jitter Measurements

Table 3. PCIe Gen 1 Jitter Data

Mode (both devices)	Measured at Output of 1st Si53112	Measured at Output of 2nd Si53112	Max Spec
Bypass mode	14.3 ps	15.3 ps	86 ps
PLL mode, High Loop BW	26.3 ps	34.9 ps	
PLL mode, Low Loop BW	28.6 ps	35.2 ps	

Table 4. PCIe Gen 2 Jitter Data

Mode (both devices)	Measured at Output of 1st Si53112	Measured at Output of 2nd Si53112	Max Spec
Bypass mode	1.38 ps rms	1.51 ps rms	3.1 ps rms
PLL mode, High Loop BW	2.5 ps rms	2.9 ps rms	
PLL mode, Low Loop BW	2.2 ps rms	2.3 ps rms	

Table 5. PCIe Gen 3 Jitter Data

Mode (both devices)	Measured at Output of 1st Si53112	Measured at Output of 2nd Si53112	Max Spec
Bypass mode	0.36 ps rms	0.4 ps rms	1 ps rms
PLL mode, High Loop BW	0.58 ps rms	0.7 ps rms	
PLL mode, Low Loop BW (both devices)	0.57 ps rms	0.62 ps rms	

3. Detailed Board Schematics

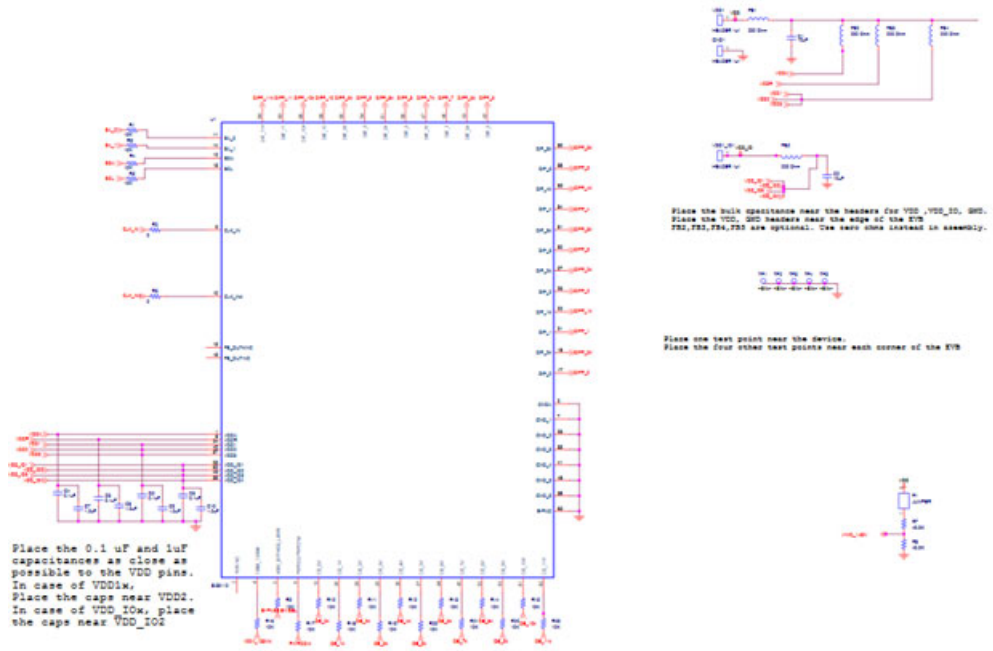

Figure 11. Schematic 1

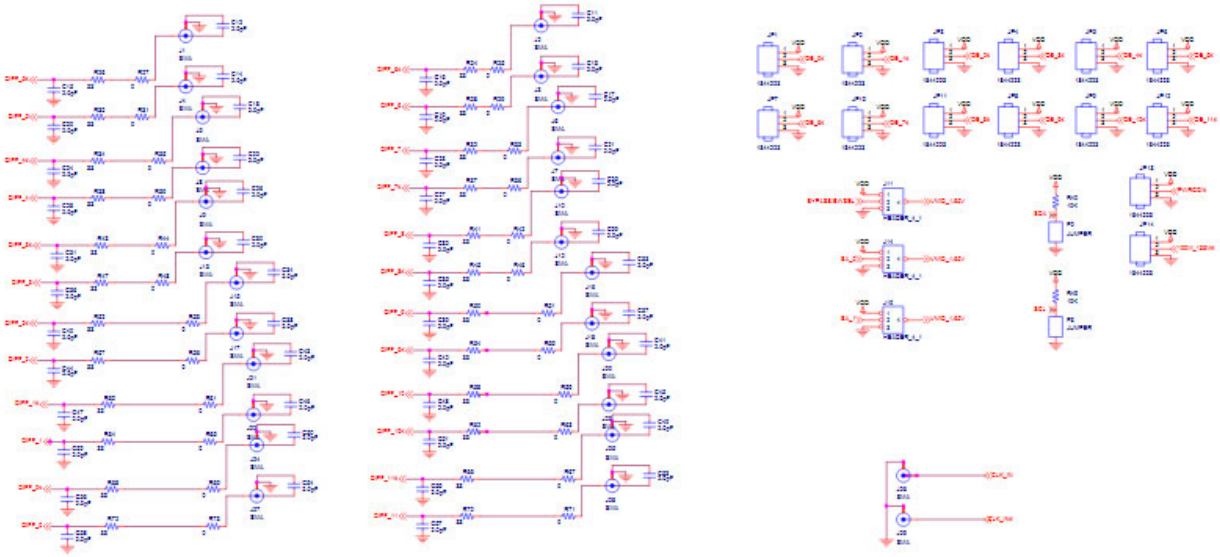

Figure 12. Schematic 2

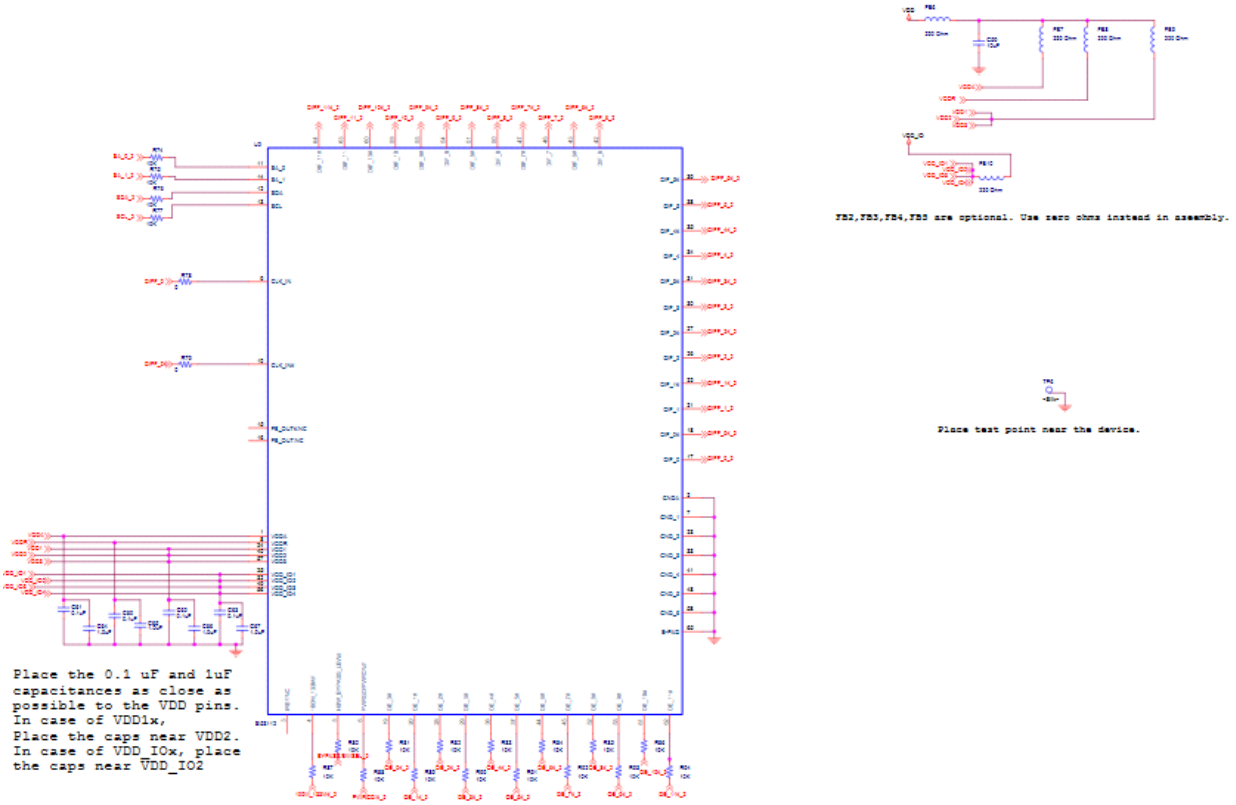

Figure 13. Schematic 3

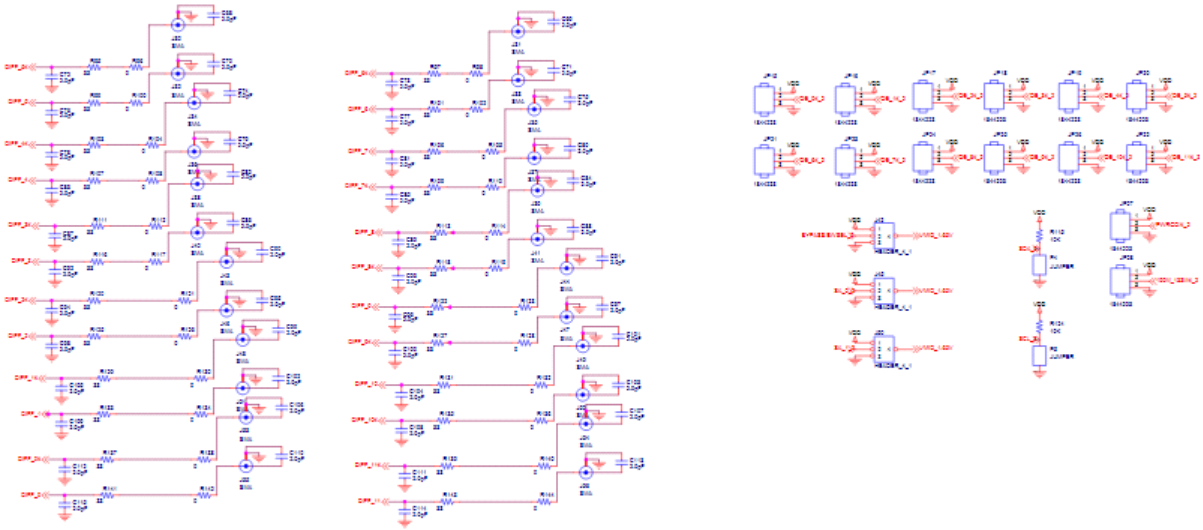

Figure 14. Schematic 4

4. Conclusion

The family of PCIe buffers noted in Table 1 offer both fanout buffer and zero-delay buffer capabilities. Fanout buffer mode presents the best jitter performance, while zero-delay buffer mode presents the best skew performance in either low loop bandwidth or high loop bandwidth modes.

All modes pass PCIe Gen1/2/3 specifications with the following characteristics:

- Fanout buffer mode provides low additive PCIe jitter and lowest overall PCIe jitter assuming a low noise reference
- ZDB mode with Low Loop BW provides the lowest intrinsic PCIe jitter
- ZDB mode with High Loop BW provides acceptable intrinsic PCIe jitter

Overall recommendation for cascading two Skyworks Solutions PCIe buffer devices are:

- Follow the schematic and design guidelines
- Choose fanout buffer mode if jitter performance is highest priority in your design
- Choose low loop BW mode if skew performance is highest priority in your design

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