
CASCADING TWO Si53112 BUFFERS

1. Introduction

It is becoming more common in server and storage applications to require more than twenty 100 MHz PCIe Gen2/3 clock outputs for various system functions and ICs. The highest output count PCIe Gen2/3 buffer available in the market provides 19 outputs, requiring board designers to cascade multiple buffers to achieve a higher number of outputs.

This application note provides schematic and design guidelines for cascading multiple Si53112 devices together, ensuring optimal input to output delay and PCIe gen jitter performance.

2. Board Design and Verification

Two concerns in cascaded PCIe clock buffer topologies are:

1. Propagation delay (from input of first buffer to outputs from the second buffer), and
2. PCIe Gen1/2/3 jitter performance.

To ensure the output clocks are within PCIe specifications in cascaded buffer topology, we have developed an evaluation board that cascades two Si53112 devices, with Si5338 being the frequency source. This board is shown in Figure 1.

The board features two types of traces:

1. Traces on the top layer in a 6-layer PCB.
2. Traces in the middle layer (layer-3) in a 6-layer PCB.

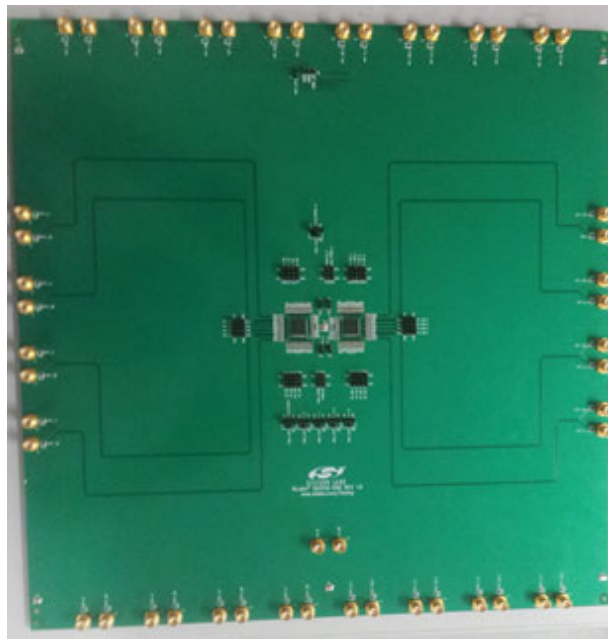


Figure 1. PCB with Two Cascaded Si53112 Devices

The board has the following design highlights:

1. Clock traces are 10 inches long for each output pair.
2. Each device has a dedicated power supply filter.
3. CLK0 output of the first device is the reference input to the second device.
4. Each device has dedicated control pins such as OE pins, BW/Bypass selection pin, etc.

The Skyworks Solutions PCIe buffers listed in Table 1 can operate in either fanout buffer or zero-delay buffer modes, and adhere to the performance specifications outlined in the DB800ZL, DB1200ZL, or DB1900Z PCIe requirements for server and storage motherboard design reference platforms.

Table 1. Skyworks Solutions PCIe Server Buffer Family

Part Number	Outputs	Output Buffer Type
Si53106	6	Push-Pull
Si53108	8	Push-Pull
Si53112	12	Push-Pull
Si53115	15	Push-Pull
Si53119	19	Push-Pull
Si53019	19	Constant Current

It should be noted that the analysis discussed in this application note is based on data taken on two cascaded Si53112 PCIe buffers; however, similar performance can be expected when cascading any two buffers noted in Table 1.

Our cascaded Si53112 test board was tested in zero-delay buffer mode (high loop band-width and low loop band-width modes), as well as fanout buffer mode. The subsequent sections present the measurement results of clock outputs in these three settings.

2.1. Signal Integrity Measurements

Table 2 shows the propagation delay (input to output skew) for various settings and Figures 2-10 show the oscilloscope shots.

Table 2. Input to Output Skew Measurements

Mode (both devices)	Skew (Input to Output of First Si53112)	Skew (Input of First to Output of Second Si53112)
Bypass mode	3.436 nS	7.108 nS
PLL mode, High Loop BW	-188.797 pS	-178.491 pS
PLL mode, Low Loop BW	-188.442 pS	-174.142 pS



Figure 2. Input Clock vs. Output Clock of 1st Si53112, Bypass Mode

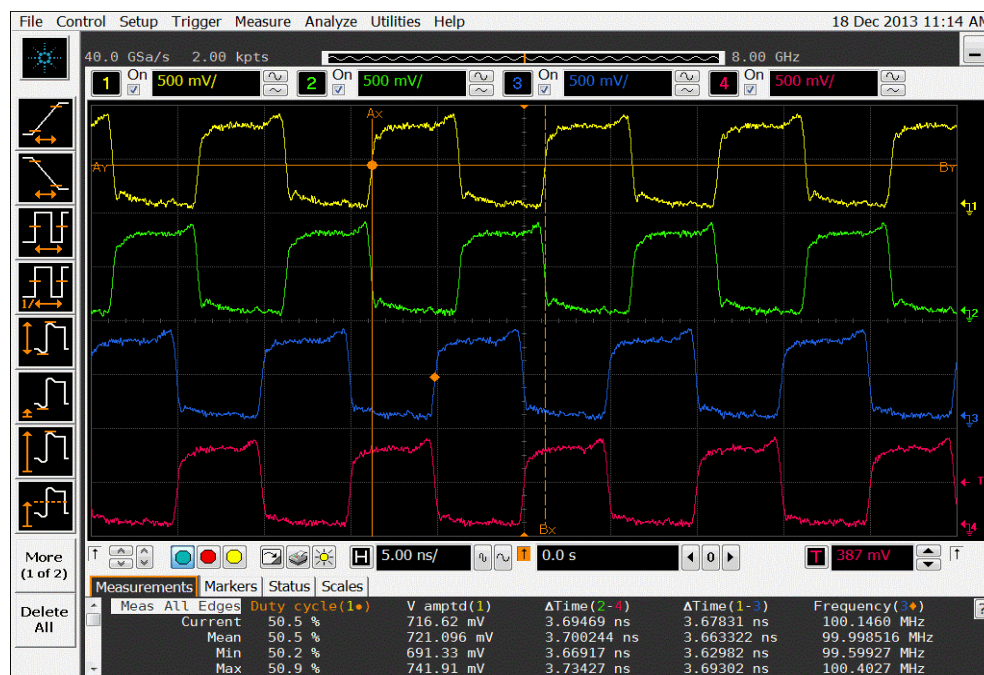


Figure 3. Output Clock of 1st Si53112 vs. Output Clock of 2nd Si53112, Bypass Mode

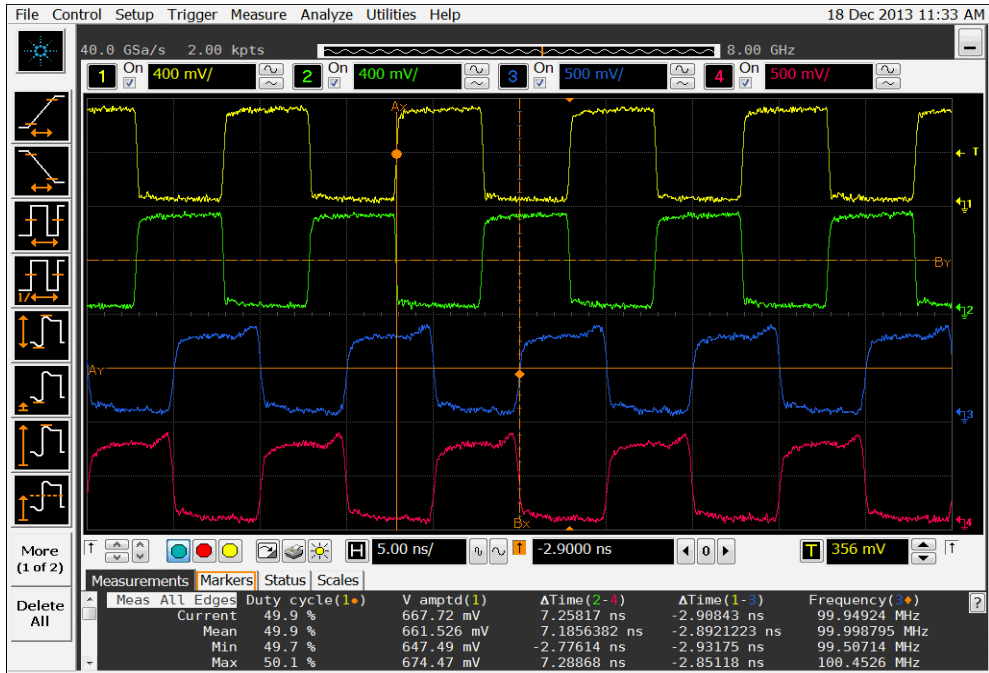


Figure 4. Input Clock vs. Output Clock of 2nd Si53112, Bypass Mode

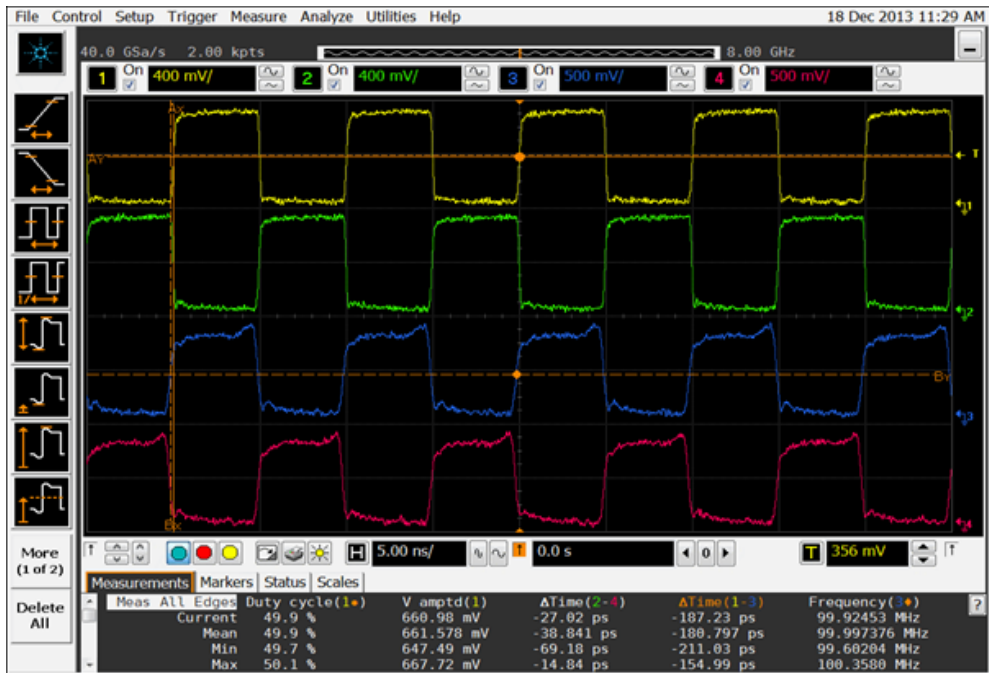


Figure 5. Input Clock vs. Output Clock of 1st Si53112, HBW PLL Mode

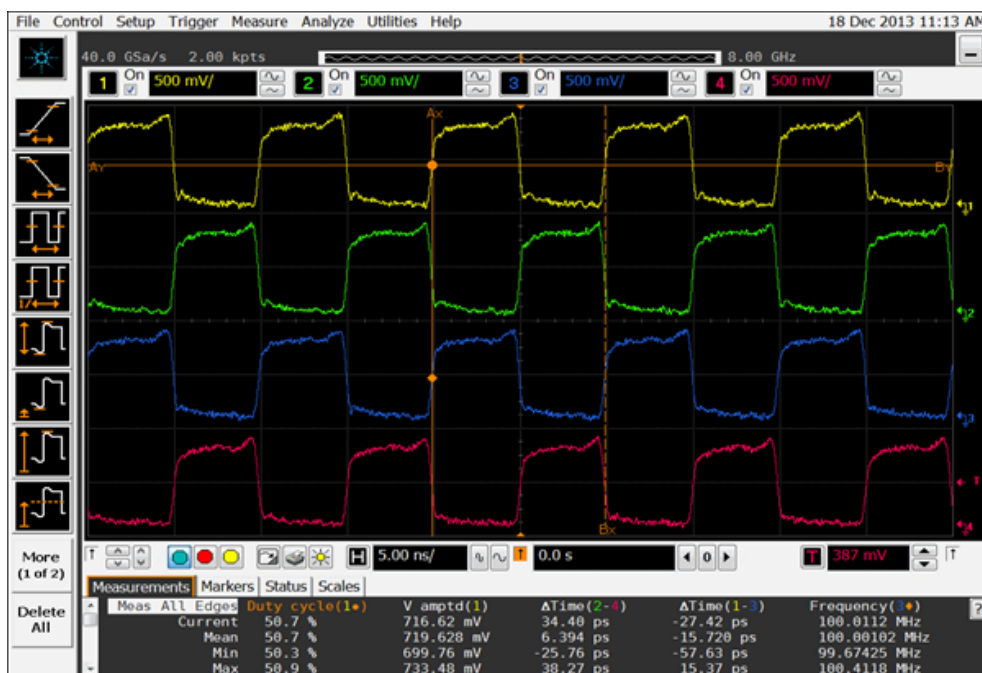


Figure 6. Output Clock of 1st Si53112 vs. Output Clock of 2nd Si53112, HBW PLL Mode

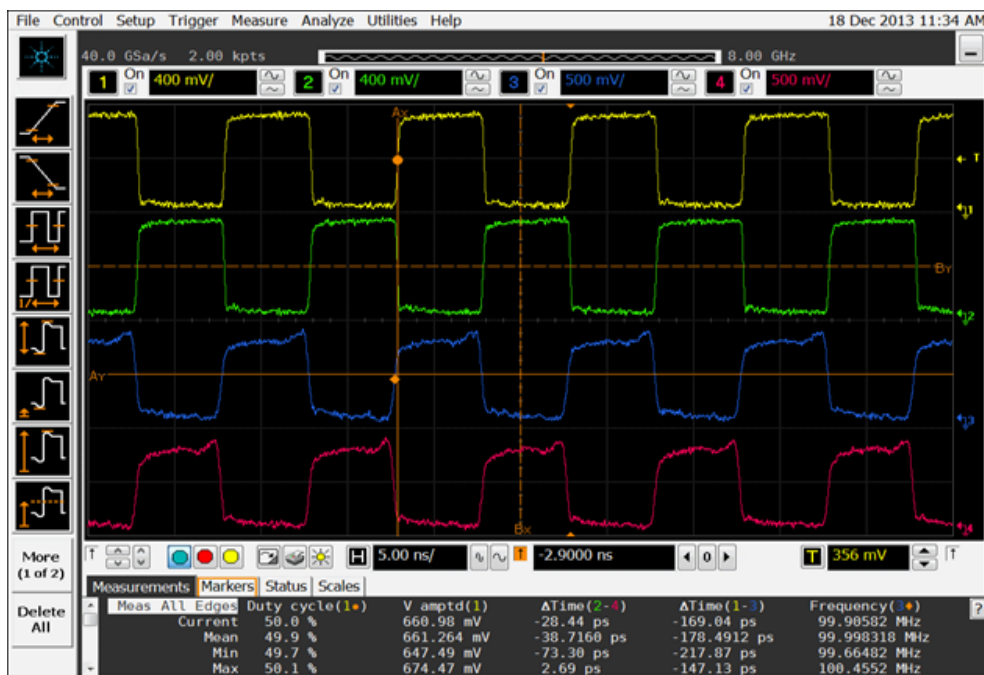


Figure 7. Input Clock vs. Output Clock of 2nd Si53112, HBW PLL Mode

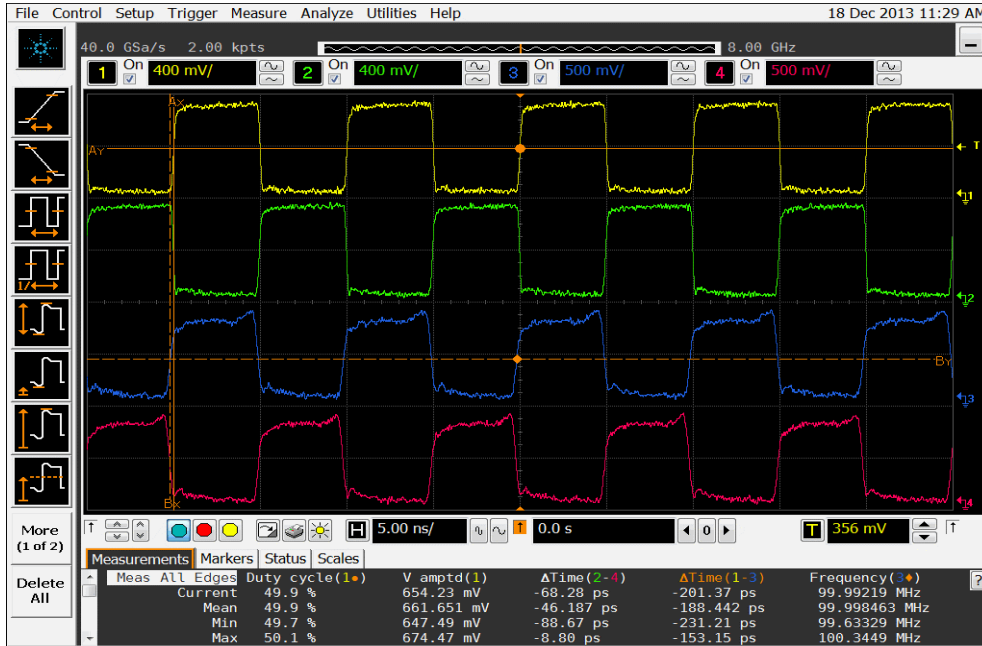


Figure 8. Input Clock vs. Output Clock of 1st Si53112, LBW PLL Mode

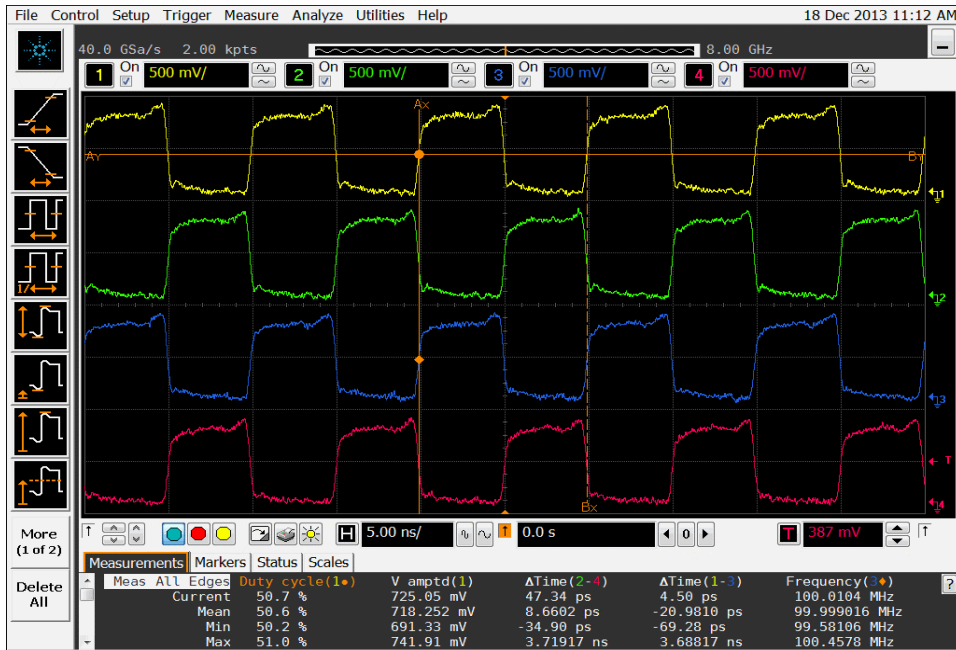


Figure 9. Output Clock of 1st Si53112 vs. Output Clock of 2nd Si53112, LBW PLL Mode



Figure 10. Input Clock vs. Output Clock of 2nd Si53112, LBW PLL Mode

2.2. PCIe Gen Jitter Measurements

Table 3. PCIe Gen 1 Jitter Data

Mode (both devices)	Measured at Output of 1st Si53112	Measured at Output of 2nd Si53112	Max Spec
Bypass mode	14.3 ps	15.3 ps	86 ps
PLL mode, High Loop BW	26.3 ps	34.9 ps	
PLL mode, Low Loop BW	28.6 ps	35.2 ps	

Table 4. PCIe Gen 2 Jitter Data

Mode (both devices)	Measured at Output of 1st Si53112	Measured at Output of 2nd Si53112	Max Spec
Bypass mode	1.38 ps rms	1.51 ps rms	3.1 ps rms
PLL mode, High Loop BW	2.5 ps rms	2.9 ps rms	
PLL mode, Low Loop BW	2.2 ps rms	2.3 ps rms	

Table 5. PCIe Gen 3 Jitter Data

Mode (both devices)	Measured at Output of 1st Si53112	Measured at Output of 2nd Si53112	Max Spec
Bypass mode	0.36 ps rms	0.4 ps rms	1 ps rms
PLL mode, High Loop BW	0.58 ps rms	0.7 ps rms	
PLL mode, Low Loop BW (both devices)	0.57 ps rms	0.62 ps rms	

3. Detailed Board Schematics

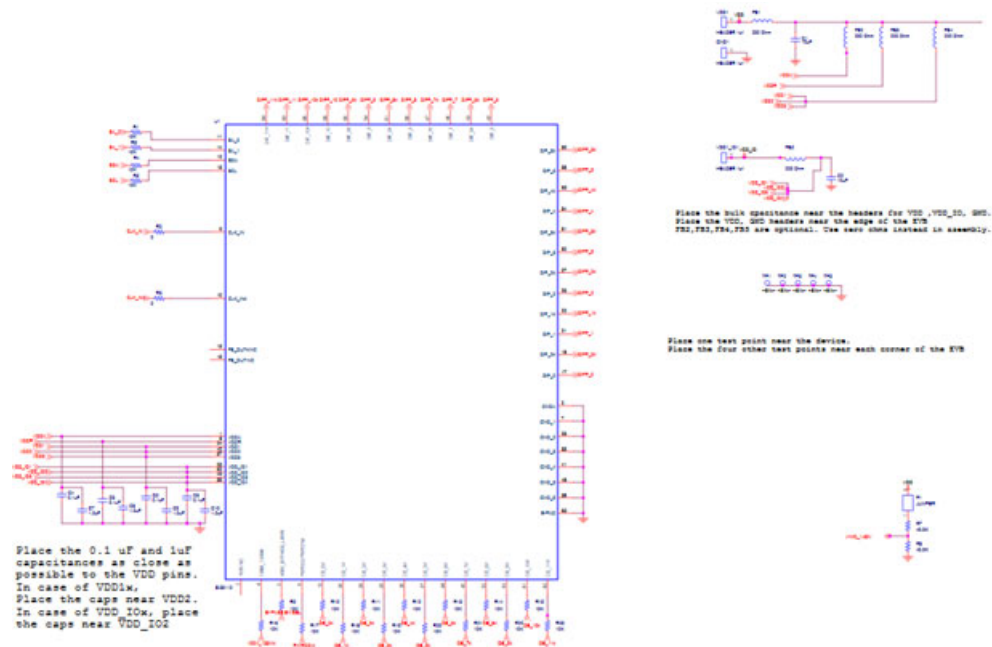


Figure 11. Schematic 1

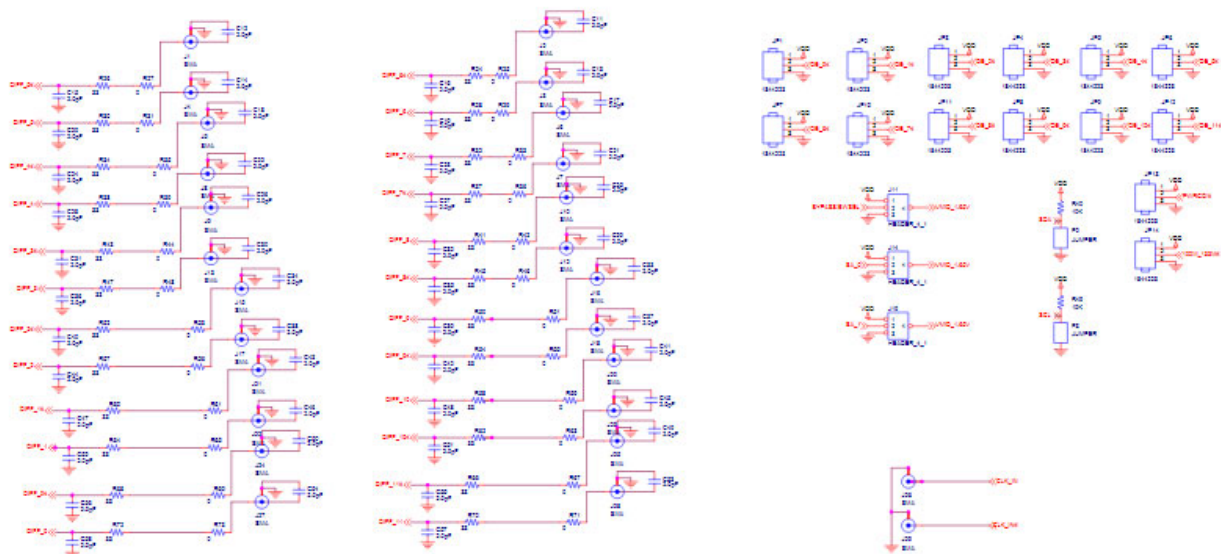


Figure 12. Schematic 2

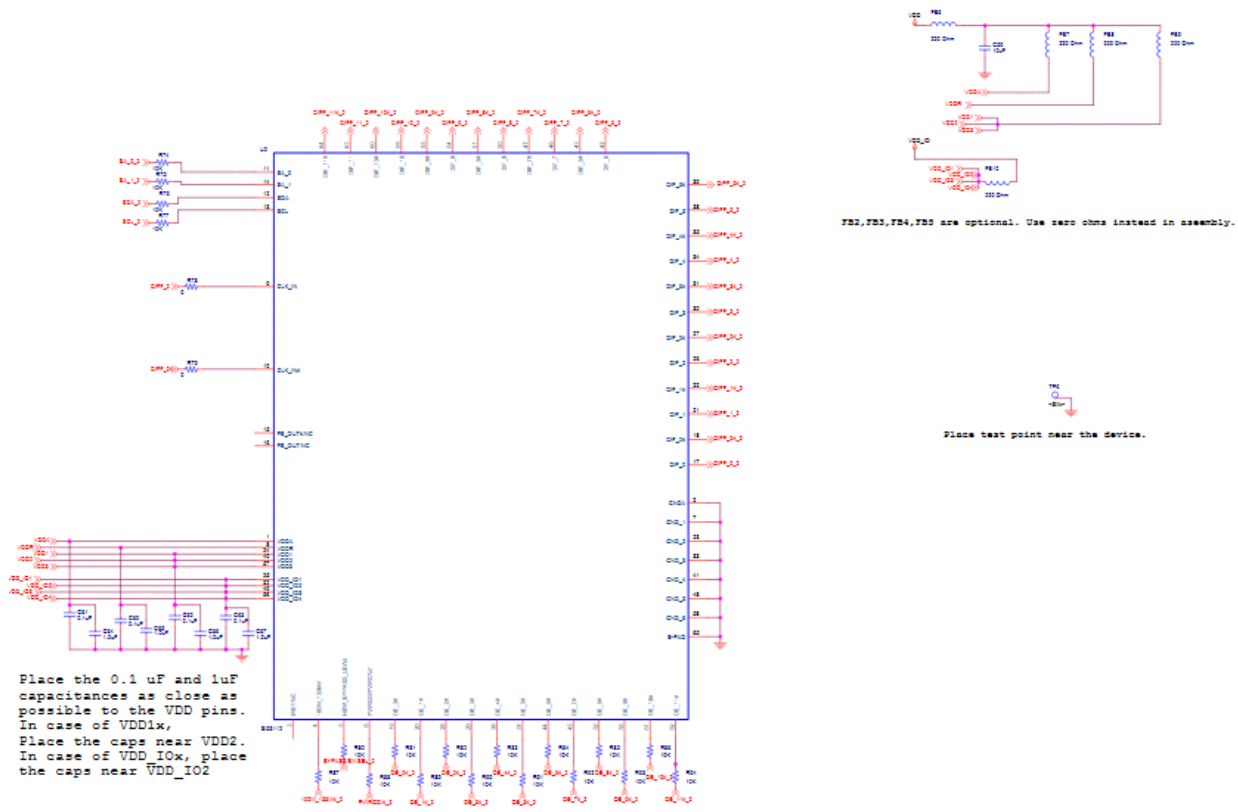


Figure 13. Schematic 3

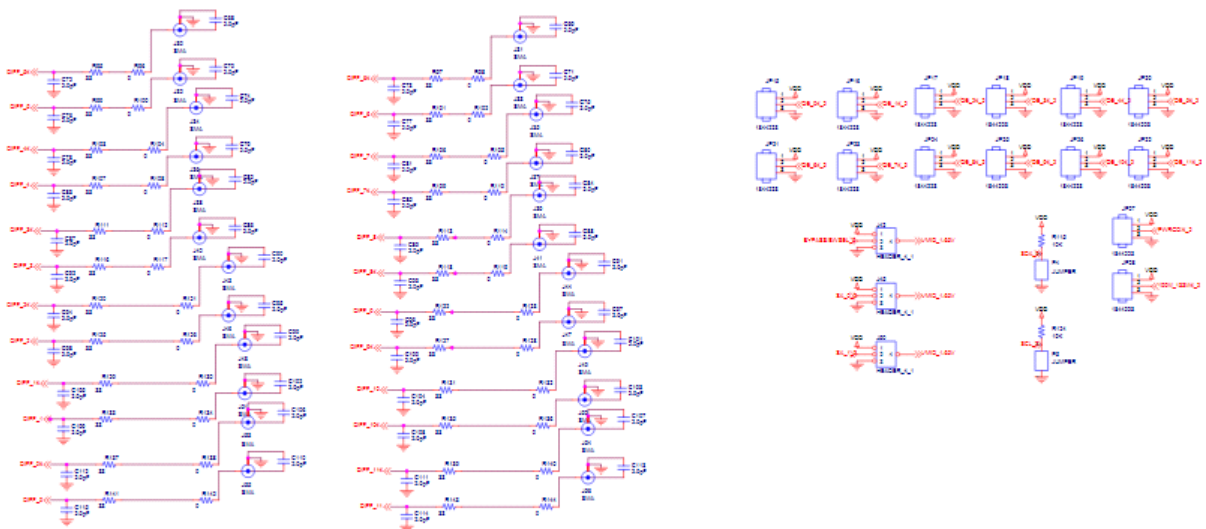


Figure 14. Schematic 4

4. Conclusion

The family of PCIe buffers noted in Table 1 offer both fanout buffer and zero-delay buffer capabilities. Fanout buffer mode presents the best jitter performance, while zero-delay buffer mode presents the best skew performance in either low loop bandwidth or high loop bandwidth modes.

All modes pass PCIe Gen1/2/3 specifications with the following characteristics:

- Fanout buffer mode provides low additive PCIe jitter and lowest overall PCIe jitter assuming a low noise reference
- ZDB mode with Low Loop BW provides the lowest intrinsic PCIe jitter
- ZDB mode with High Loop BW provides acceptable intrinsic PCIe jitter

Overall recommendation for cascading two Skyworks Solutions PCIe buffer devices are:

- Follow the schematic and design guidelines
- Choose fanout buffer mode if jitter performance is highest priority in your design
- Choose low loop BW mode if skew performance is highest priority in your design



SKYWORKS®

ClockBuilder Pro

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

www.skyworksinc.com/CBPro



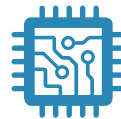
Portfolio

www.skyworksinc.com/ia/timing



SW/HW

www.skyworksinc.com/CBPro



Quality

www.skyworksinc.com/quality



Support & Resources

www.skyworksinc.com/support

Copyright © 2021 Skyworks Solutions, Inc. All Rights Reserved.

Information in this document is provided in connection with Skyworks Solutions, Inc. ("Skyworks") products or services. These materials, including the information contained herein, are provided by Skyworks as a service to its customers and may be used for informational purposes only by the customer. Skyworks assumes no responsibility for errors or omissions in these materials or the information contained herein. Skyworks may change its documentation, products, services, specifications or product descriptions at any time, without notice. Skyworks makes no commitment to update the materials or information and shall have no responsibility whatsoever for conflicts, incompatibilities, or other difficulties arising from any future changes.

No license, whether express, implied, by estoppel or otherwise, is granted to any intellectual property rights by this document. Skyworks assumes no liability for any materials, products or information provided hereunder, including the sale, distribution, reproduction or use of Skyworks products, information or materials, except as may be provided in Skyworks' Terms and Conditions of Sale.

THE MATERIALS, PRODUCTS AND INFORMATION ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, INCLUDING FITNESS FOR A PARTICULAR PURPOSE OR USE, MERCHANTABILITY, PERFORMANCE, QUALITY OR NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHT; ALL SUCH WARRANTIES ARE HEREBY EXPRESSLY DISCLAIMED. SKYWORKS DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. SKYWORKS SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING BUT NOT LIMITED TO ANY SPECIAL, INDIRECT, INCIDENTAL, STATUTORY, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS THAT MAY RESULT FROM THE USE OF THE MATERIALS OR INFORMATION, WHETHER OR NOT THE RECIPIENT OF MATERIALS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Skyworks products are not intended for use in medical, lifesaving or life-sustaining applications, or other equipment in which the failure of the Skyworks products could lead to personal injury, death, physical or environmental damage. Skyworks customers using or selling Skyworks products for use in such applications do so at their own risk and agree to fully indemnify Skyworks for any damages resulting from such improper use or sale.

Customers are responsible for their products and applications using Skyworks products, which may deviate from published specifications as a result of design defects, errors, or operation of products outside of published parameters or design specifications. Customers should include design and operating safeguards to minimize these and other risks. Skyworks assumes no liability for applications assistance, customer product design, or damage to any equipment resulting from the use of Skyworks products outside of Skyworks' published specifications or parameters.

Skyworks, the Skyworks symbol, Sky5®, SkyOne®, SkyBlue™, Skyworks Green™, Clockbuilder®, DSPLL®, ISOModem®, ProSLIC®, and SiPHY® are trademarks or registered trademarks of Skyworks Solutions, Inc. or its subsidiaries in the United States and other countries. Third-party brands and names are for identification purposes only and are the property of their respective owners. Additional information, including relevant terms and conditions, posted at www.skyworksinc.com, are incorporated by reference.

Skyworks Solutions, Inc. | Nasdaq: SWKS | sales@skyworksinc.com | www.skyworksinc.com

USA: 781-376-3000 | Asia: 886-2-2735 0399 | Europe: 33 (0)1 43548540 |  