

# AN952: PCIe Jitter Estimation Using an Oscilloscope

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Jitter of the reference clock has a direct impact on the efficiency of the data transfer between two PCIe devices. The data recovery process is able to track a portion of the jitter frequencies that are within its bandwidth, but the untrackable jitter frequencies must be limited. This untrackable jitter spectrum is defined using a series of transfer functions that represent the loop bandwidths of the PLLs and the CDR that affect the data recovery process. Each PCIe standard defines its overall transfer function, parameters (e.g. loop bandwidth), and jitter limits. Using these parameters, we are able to estimate the contribution of the untrackable jitter using an oscilloscope. However, due to an oscilloscope limitation, the results will only provide a reasonable estimate to whether a device will pass a specific PCIe standard.

**Note:** For full compliance testing for a PCIe standard, all defined bandwidth and transfer functions must be met. This guide is only meant to provide an estimation. To determine full compliancy, use the [Skyworks Clock Jitter Tool](#).

The following sections will show how to set up an oscilloscope according to the parameters defined for each PCIe standard, and discuss why only certain standard specifications can be measured using an oscilloscope.

## KEY POINTS

- Discusses the limitations of measuring PCIe reference clock jitter with an oscilloscope.
- Explains why reference clock jitter for PCIe Gen 2.1 cannot be measured.
- Provides instructions on configuring the oscilloscope based on PCIe standards.
- Provides oscilloscope setup files and example measurement captures.

## 1. Limitations when Measuring PCIe with an Oscilloscope

For the Common Refclk RX Architecture, each PCIe standard is defined by an overall jitter transfer function made up of:

$$\text{Transmit Path/Tx PLL: } H_1(s) = \frac{(2s\zeta_1\omega_{n1} + \omega_{n1}^2)}{(s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2)}$$

$$\text{Receive Path/Rx PLL: } H_2(s) = \frac{(2s\zeta_2\omega_{n2} + \omega_{n2}^2)}{(s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2)}$$

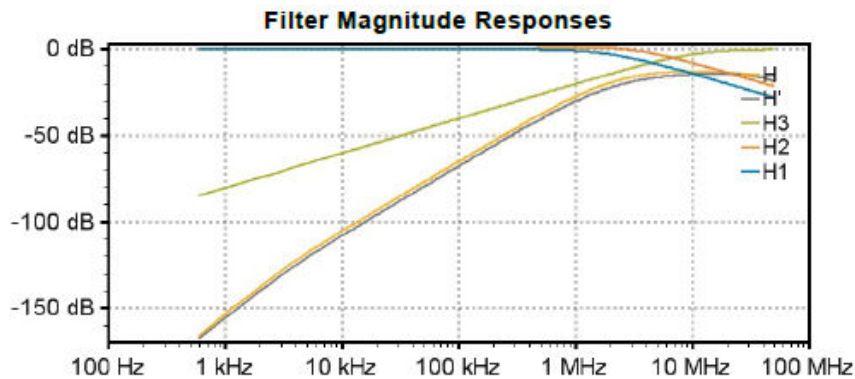
$$\text{CDR: } H_3(s) = \frac{s}{(s + \omega_{n3})}$$

To accurately define the overall jitter transfer function, the oscilloscope needs the capability to define each of the individual transfer functions. However, due to the current oscilloscope technology, only a single transfer function can be defined limiting our capability to fully define the overall transfer function. To compensate for this limitation, approximations to the individual transfer functions can be made allowing us to define the overall transfer function using a single PLL. These approximations provide reasonable untracked jitter contribution results, which allow us to estimate if the device will pass either PCIe Gen 1.1 or PCIe Gen 3.0.

**Note:** The same assumptions mentioned above for PCIe Gen 1.1 and 3.0 cannot be applied to Gen 2.1.

To estimate PCIe Gen 1.1 and Gen 3.0 jitter with an oscilloscope, the following approximations are made:

1. Either  $\omega_{n1} \gg \omega_{n2}$  or  $\omega_{n2} \gg \omega_{n1}$  allowing the difference between transmit and receive paths to be approximated as either  $H_1(s)-1$  or  $1-H_2(s)$ . For example, the below PCIe Gen 3.0 specification can be measured because  $\omega_{n2} = 11.53 \text{ Mrad/s} \gg \omega_{n1} = 0.448 \text{ Mrad/s}$ .
2. The CDR transfer function cutoff frequency is large enough that the CDR contribution will be minimal, i.e.,  $H_3(s) \approx 1$ . Looking at the below PCIe Gen 3.0 magnitude response, we can see the CDR's high pass filter response will have minimal effect on the overall jitter transfer function, H.
3. The REFCLK Path Delay Difference, T, is negligible.
4. The clock will be unaffected if the Tx PLL has a high bandwidth allowing  $H_1(s) \approx 1$ .



**Figure 1.1. PCIe Gen3.0 Filter Magnitude Response Generated From Skyworks PCIe Clock Jitter Tool**

**Note:** For the figure above, measurements are: PLL1 BW = 2 MHz, PLL1 Peaking = 0.01 dB, PLL2 BW = 5 MHz, PLL2 Peaking = 1 dB.

### 1.1 Why PCIe Gen 2.1 Cannot be Measured

PCIe Gen2.1 cannot be measured because the difference between each path's cutoff frequencies ( $\omega_{n1} = 0.896 \cdot 2\pi$  Mrad/s vs.  $\omega_{n2} = 4.31 \cdot 2\pi$  Mrad/s) is not large enough for one path to dominate the other, as in the first approximation above. Therefore both  $H_1(s)$  and  $H_2(s)$  must be defined, which is not possible with the current oscilloscope technology being limited to only specifying a single transfer function. If the same assumptions are made as above, the defined overall transfer function would not account for a portion of the untracked jitter highlighted below.

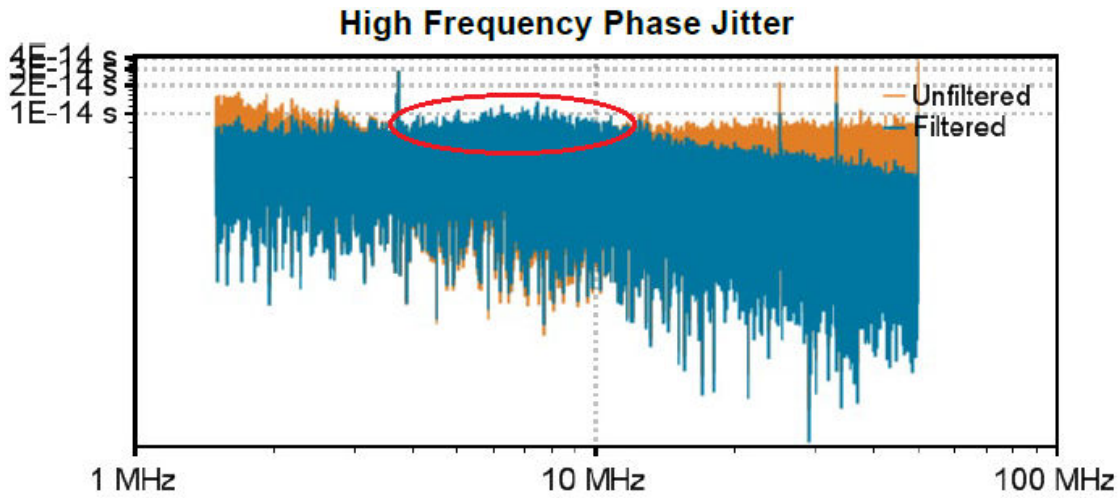


Figure 1.2. PCIe Gen 2.1 High Frequency Phase Jitter

**Note:** For the figure above, measurements are: PLL1 BW = 8 MHz, PLL1 Peaking = 3 dB, PLL2 BW = 16 MHz, PLL2 Peaking = 1 dB.

## 2. Configuring Oscilloscope

The following section describes how to measure PCIe jitter based on the parameters outlined in each PCIe standard's transfer function. The test platform used for the measurements was a Skyworks Si5338 Evaluation Board (EVB). The Si5338 was set to output a 100 MHz HCSL signal from CLK0 based on the PCIe standard driver requirements. Two 50  $\Omega$  SMA cables were then used to connect DIFF0 and DIFF0# to CH1 and CH2 of a Keysight DSA90804A oscilloscope.

### 2.1 Manually Configure Oscilloscope

For the purpose of this application note, the PCIe Gen 3.0 Common Clock RX Architecture specification outlined in [Figure 1.1 PCIe Gen3.0 Filter Magnitude Response Generated From Skyworks PCIe Clock Jitter Tool on page 2](#) will be measured.

1. The two single-ended inputs on CH1 and CH2 need to be combined to create a differential signal. To create the differential signal, the oscilloscope's math settings can be used to subtract CH2 from CH1. From the default window, select "Math" → "Function", and the window below will appear.



Figure 2.1. Creating a Differential Signal Using the Math Function (Part 1)

Under Function 1, select "Math" → "Subtract", and set the two sources to Channel 1 and Channel 2. From here, check the "On" box to display the new differential signal.



Figure 2.2. Creating a Differential Signal Using the Math Function (Part 2)

2. Once the differential signal has been created, the observation window of the oscilloscope needs to be configured. The following settings were chosen for performance and to clearly display the waveform.

- Time Base: 40  $\mu$ s/div
- Voltage Setting: 100 mV/div
- Sampling Rate (min): 40 GSa/s
- Sampling Bandwidth: 8.0 GHz

Once the observation window has been properly configured, the following waveform will appear.



Figure 2.3. Example Waveform

3. Once the waveform is properly displayed, a TIE filter is applied to specify the bounds of the untracked jitter contribution and to provide a means for measuring RMS phase jitter. To select a TIE filter, go to "Measure" → "Jitter/Noise" → "Advanced" → "TIE Filter".



Figure 2.4. Add TIE Measurement



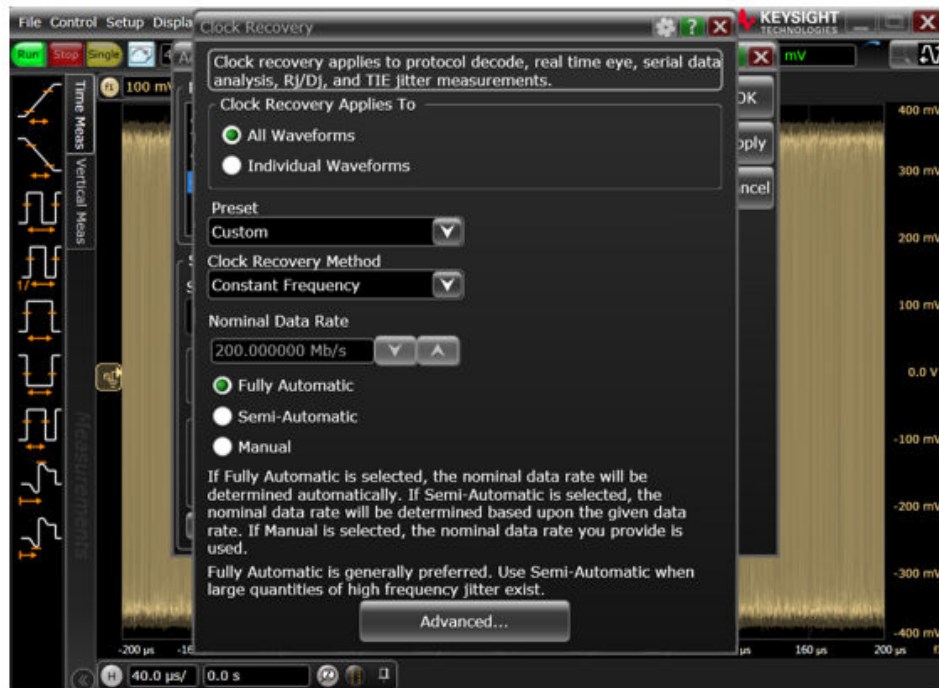
- After the TIE Filter has been selected, the filter cutoffs can be entered. Enter the desired start and stop frequency values based on the parameters specified by the PCIe standard. For this example, the TIE filter will be applied from 4 MHz to 50 MHz.



**Figure 2.5. Specify TIE Filter**

- Once the bounds of the untracked jitter have been specified using a TIE filter, the overall jitter transfer function can be applied. To apply the overall jitter transfer function, the Clock Recovery feature will be used to create either the transmit path,  $H_1(s)$ , or the receive path,  $H_2(s)$ .

From the Jitter/Noise setup window, select "Clock Recovery" and the following window will appear.



**Figure 2.6. Clock Recovery Default**

6. In the Clock Recovery window, we are able to specify the remaining overall transfer function parameters. First, under "Clock Recovery Method", select "Second Order PLL". Once selected, the below screen should appear where we can now enter the remaining parameters. Select "JTF" (Jitter Transfer Function) and enter the Loop Bandwidth and Peaking parameters. As discussed above, to create an approximation choose either  $H_1(s)$  or  $H_2(s)$  parameters based on the larger cutoff frequency. For our example, Loop Bandwidth = 2 MHz and Peaking = 1.0 dB.

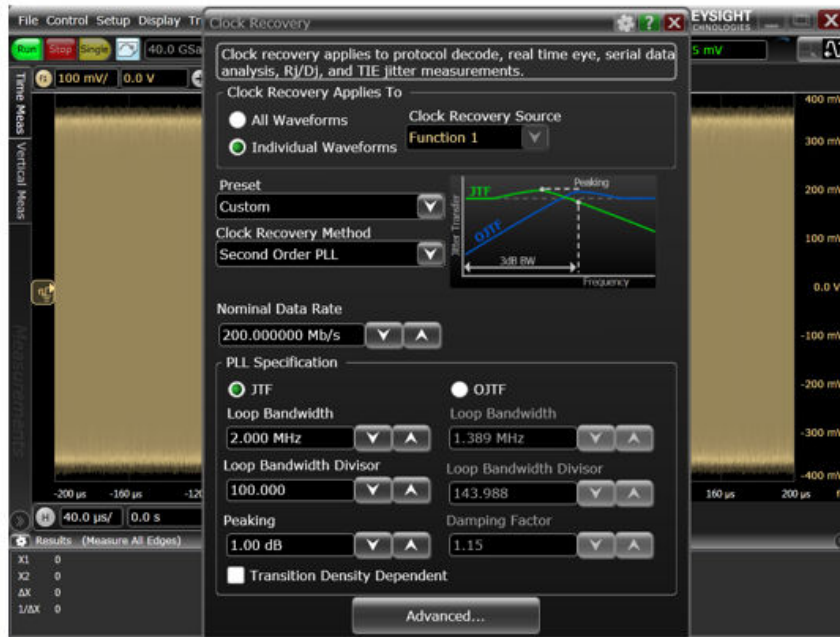


Figure 2.7. Example PCIe Gen 3.0 Clock Recovery Settings

7. Once everything is set, return to the jitter tab, select "Enable", and the following image will appear with our newly applied PCIe Gen 3.0 measurement.



Figure 2.8. Example PCIe Gen 3.0 Scope Capture



8. Once the overall transfer function has been applied, we can compare our results against the PCIe Common Refclk RX Architecture Limits in the table below to see if the device has passed. Each PCIe standard specifies its jitter requirements slightly differently, so the correlation between the oscilloscope measurement and standard requirements is important to understand.

The oscilloscope configuration allows us to quickly read off the measured jitter values to estimate whether the device will pass PCIe Gen 1.1 ( $DJ_{pk-pk}$ ) or Gen 3.1 ( $PJ_{RMS}$ ).

**Table 2.1. Common RefCLK Rx Architecture Limits**

	Description	Symbol	Limit	Units
<b>PCIe 1.1</b>	Random Jitter	$R_j$	4.7	ps pk-pk
	Deterministic Jitter	$D_j$	41.9	ps pk-pk
<b>PCIe 2.1</b>	Total Jitter where $T_j = D_j + 14.069 \times R_j$ (for BER $10^{-12}$ )	$T_j$	108	ps pk-pk
	High Frequency RMS Jitter Measured from 1.5 MHz to Nyquist (or $f_{REFCLK} / 2$ )	$J_{RMS-HF}$	3.1	ps RMS
	Low Frequency RMS Jitter Measured from 10 kHz to 1.5 MHz	$J_{RMS-LF}$	3.0	ps RMS
<b>PCIe 3.1</b>	Low Frequency RMS Jitter Measured from 10 kHz to 1.5 MHz	$J_{RMS-LF}$	3.0	ps RMS
	Random Jitter	$J_{RMS}$	1.0	ps RMS
<b>Note:</b>				
1. RefCLK Rx architecture limits are from AN562: "PCIe Express 3.1 Jitter Requirements".				

## 2.2 Using Setup Files

If the Keysight DSA90804A oscilloscope is available in your lab for testing, Skyworks has provided the necessary setup files for PCIe Gen1.1 and Gen 3.0 testing. The preconfigured setup files can be found [here](#).

To run a test using the setup files, ensure that CLK+ and CLK- are connected to CH1 and CH2 of the DSA. Then load the desired PCIe standard setup file. The following waveform should be obtained. Refer back to [Table 2.1 Common RefCLK Rx Architecture Limits on page 9](#) for the Common Refclk RX Architecture jitter requirements.



Figure 2.9. Capture Waveform Using PCIe Gen 3.0 Setup File

### 2.3 Example Scope Measurements

An example for each generation of PCIe standard is shown below. The remaining plots for each PCIe standard can be found at: <https://www.skyworksinc.com/en/application-pages/pcie-clock-jitter-tool>.



Figure 2.10. PCIe Gen 1.1 Results



Figure 2.11. PCIe Gen 3.0 Results

**Note:** Measurements for PCIe Gen 3.0 above are: PLL1 BW = 4 MHz, PLL1 Peaking = 0.01 dB, PLL2 BW = 2 MHz, PLL2 Peaking = 1 dB.

### 3. Conclusion

Based on the transfer function parameters defined by each PCIe standard, we are able to use an oscilloscope to measure the untracked jitter contribution. However, due to current oscilloscope technology only having the ability to define a single PLL, the described method is only able to provide a quick, reasonable estimate as to whether a device will pass either PCIe Gen 1.1 or PCIe Gen 3.0.



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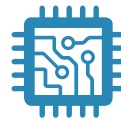
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