TSM-23-0054

Advanced Process Monitoring through Fault Detection and Classification for the Process Development of Tantalum Nitride Thin Film Resistors

Stephanie Y Chang, Shiban Tiku, and Lam Luu-Henderson

Abstract—**This paper discusses the optimization of an advanced process monitoring scheme with interdicting fault detection and classification (FDC) capabilities that improved the control over the process development of Tantalum Nitride thin film resistors (TaN TFR). Its implementation in a high-volume manufacturing environment resulted in a reduction of misprocessed wafers, shorter equipment downtime, higher throughput, enhanced process visibility, and yield improvement. Along with optimizing FDC capabilities, implementing a short loop sampling plan reduced the turnaround time for early electrical characterization by a factor of four; this allowed for timely inline adjustments within the fabrication process to tighten the statistical process control (SPC) over the distribution of the process control monitor (PCM) TaN resistor value and improve thin film uniformity.**

Index Terms— **TaN, TFR, SPC, PCM, FDC, Machine Learning**

I. INTRODUCTION

Achieving the intended consistent device performance is frequently limited by the challenges and manufacturing variation faced during the fabrication. Process variation and manufacturability play key roles in determining whether the design can be manufactured within the tight tolerance of the product specifications. Nevertheless, it is crucial that manufacturing capabilities can consistently meet the defined specifications that are used during the research and development stages to validate and verify their designs when performing simulations with accurate models. For integrated circuit (IC) applications of III-V semiconductors, particularly for cutting-edge power amplifiers and high-density mixed signal designs, it is necessary to tighten the control over the process development of the TaN thin film resistor (TFR) [1], [2].

Real-time data analysis and diagnosis of detected faults within the process data are powerful tools to enhance the quality and statistical process control (SPC) in a high-volume production environment [3]. Our previous study addressed the various benefits achieved through deploying the initial stages of fault detection and classification (FDC) for in-situ process monitoring to tackle various challenges faced by the device fabrication of TaN TFR [4]. Since then, additional reports have been set up to monitor the analysis health and process metrics by FDC.

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In addition to tracking process capability indices for each process parameter, further data collection and analysis of equipment performance indicators (EPI), maintenance indicators (MI), state indicators (SI), figure of merits (FOM) have been performed. This work dives into a comprehensive study of how the advanced process monitoring scheme has been optimized to enhance the process visibility of the equipment and process behavior for TaN reactive sputtering. To ensure the reproducibility of the results for a comprehensive assessment, the scope of the data sets for process monitoring and characterization were collected from wafer runs that were processed with different tantalum (Ta) targets, in separate sputtering chambers, and at different stages of the Ta targets' life cycles. Robust statistical process control over the manufacturability of TaN TFR targeting a sheet resistance (R_s) of 50 ohms/sq, low TCR, and high intra-wafer uniformity was achieved. Advantages gained through statistical analyses, interdicting capabilities, and process tracking and utilization reports are also explored.

II. TAN REACTIVE SPUTTERING

A. Inherent Challenges

Proper conditioning of the Ta target and process chamber after performing preventative maintenance (PM) is essential to minimize intra-wafer, across-cassette, and run-to-run uniformity of the sputtered thin film. In addition to timely reassessments of the chamber and shielding conditions, it is necessary for stringent process monitoring of the "burn-in" and deposition sequences used to prepare the chamber before running product wafers. Proper conditioning of the chamber improves process stability by preventing erratic trends in inline electrical data for the TaN TFR [5].

The TaN reactive sputtering process takes place in a high vacuum chamber, in which argon (Ar) atoms are bombarded against the Ta target. As shown in Figure 1, the subsequent reaction between the Ta atoms and nitrogen ions forms a sputtered thin metal-nitride film on the substrate over time. A combination of multiple factors, such as the gas plasma, magnetic field, atom bombardment, ratio of process gases, and Ta target's wear pattern can heavily influence the intra-wafer uniformity. At the end of the Ta target's life cycle, the degraded uniformity signature is most apparent and causes the sputtered TaN thin films to have alternating rings of high and low R_s as shown in Figure 2. The inline SPC data in Figure 3 was

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collected from inline monitoring wafers that were processed in various sputtering chambers. Studying the trends from extensive data sets collected over several Ta targets' life cycles, higher %sigma and range values consistently corresponded to wafers that had been processed in a sputtering chamber which had a Ta target with a high kWh-based utilization percentage. Therefore, over the course of the Ta target's life cycle, the ability to detect anomalies in process trends becomes increasingly essential.

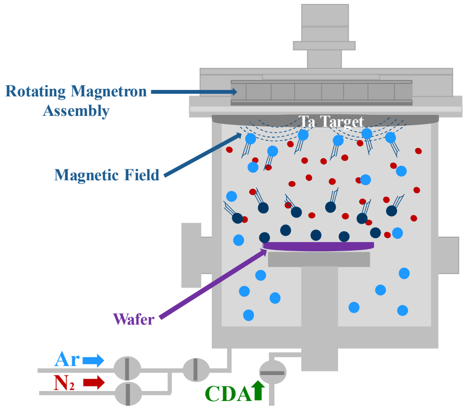

Fig. 1. Reactive sputtering process for deposited TaN thin films

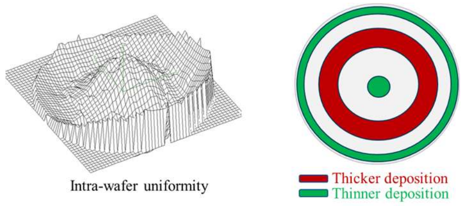

Fig. 2. Ta target's wear pattern with a prominent "sombrero" signature influences the sputtered thin film's intra-wafer uniformity and sheet resistance variation.

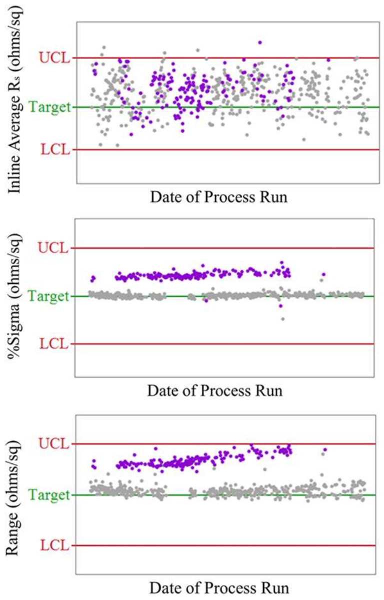

Fig. 3. Inline TaN data highlighted in purple corresponds to a sputtering chamber with a heavily used Ta target that was nearing its end of life cycle. Higher %sigma and range values trend near the upper control limit indicative of poorer intra-wafer uniformity of the sputtered thin film.

III. FAULT DETECTION AND CLASSIFICATION

A. Process Parameter Excursions

In-situ process monitoring at a run-to-run basis allows correlations to be drawn between process data and wafers that failed to meet product specifications. When a parameter excursion is detected by one of the reports, the FDC system's interdicting capabilities immediately halt the tool from processing additional wafers. Reports and models were set up to monitor analysis and process faults for a variety of parameters (e.g., cryogenic and platen temperatures, deposition power, deposition time, voltage, current, chamber pressure, process gas flow rates). Extensive data sets captured the analyses that were applied to every wafer processed in the sputtering chambers. This minimizes the risk of producing large quantities of wafer scrap that would result from issues which the tool may not alarm for.

As shown in Figure 4, the time series plot provides a snapshot of which sputtering chambers recently experienced process faults. SPC charts for inline TaN data are closely monitored for shifts and abnormal trends to establish correlations with detected parameter excursions. Identifying trends of out-of-control (OOC) process parameters flagged by FDC allowed for improvements in maintaining the health of the tool. For instance, tracking the pareto of alarms associated with the cryogenic temperature helped to define PM schedules for performing different levels of cryopump regeneration. While most trapped gasses are Ar and N_2, other gasses such as hydrogen (H_2) require more rigorous levels of cryopump regeneration for their removal. FDC helped to minimize the occurrences of aborted process runs and unexpected equipment downtime that would result from tool issues related to the cryopumps.

Instantaneous feedback achieved through FDC monitoring of process trends helped to identify sources of process variation. This allowed for tightened control over critical process parameters; this is especially crucial since the intrinsic nature of sputtering makes it difficult to control the directionality of the sputtered material during deposition and Ar can be trapped in the thin film. For instance, the wider distribution of Ar gas flow rates from a specific sputtering chamber's mass flow controller in Figure 5 correlated to higher variation in the intra-wafer uniformity and erratic inline R_s. Monitoring the base pressure before deposition ensures that the appropriate vacuum level is achieved; this prevents contaminants from being incorporated in the thin film during the sputter process and the formation of unwanted surface oxides.

Furthermore, the analysis health metrics summary report provided insight on fine-tuning SPC limits by evaluating whether the defined specifications were able to accurately

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monitor each parameter based on the process trends and flag for true excursions. Process capability indices were automatically computed for each parameter to assess the relative improvement of the monitored process.

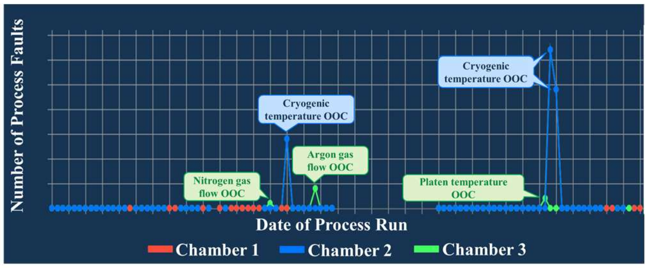

Fig. 4. Time series plot of several process faults for various monitored parameters that were flagged when wafers were being processed in the sputtering chambers.

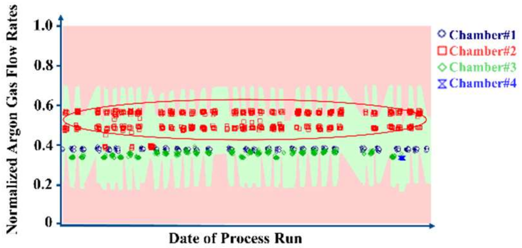

Fig. 5. Dynamic target hold x-bar set report tracked the standard deviation of charted residuals for the Ar gas flow rate from each sputtering chamber during the thin film deposition process. Chamber#2 shows higher variation in the Ar gas flow rates.

For risk assessment, wafers flagged by FDC for OOC process parameters during the sputtering process were collectively sorted into a list and reviewed for dispositioning. This streamlined the down-selection of wafers submitted to a short-loop sampling plan (M1TEST) that reduces the average turnaround time for electrical characterization of critical resistor parameters by 4X as shown in Figure 6 [6]. This electrical testing takes place after the oxidative and thermal ash treatment stabilizes the TaN TFR by bombarding the negatively charged TaN surface with positive ions in Figure 7. The Process Control Monitor (PCM) TaN R_s distributions measured after the ash treatment and at the end of the frontside process are highly correlated as shown in Figure 8. Therefore, the M1TEST provides an accurate prediction to quickly react on making necessary inline adjustments to improve the targeting of the critical PCM resistor parameters without waiting for electrical data from the end of the frontside process. Due to the drift of the PCM resistor value over time, early feedback data through M1TEST is necessary for timely reactive inline adjustments to the photo and thin film deposition steps at the resistor layer; this allows proper compensation of the process to retarget and tighten the distribution of these critical resistor parameters.

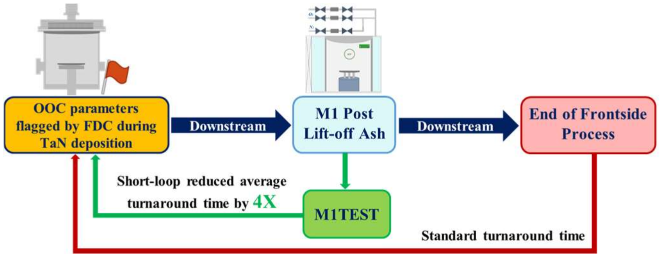

Fig. 6. A short-loop (M1TEST) for earlier electrical characterization of TaN parameters was implemented to closely monitor for process drifts.

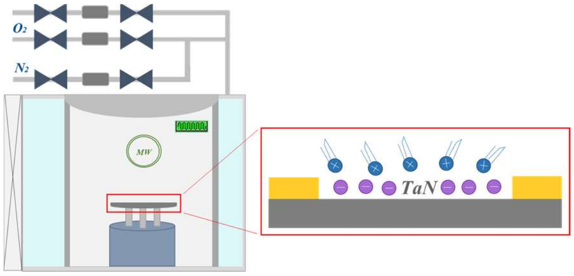

Fig. 7. Highly oxidative and thermal ash treatment bombards TaN thin film's surface to remove resist residues after metal 1 (M1) deposition and lift-off.

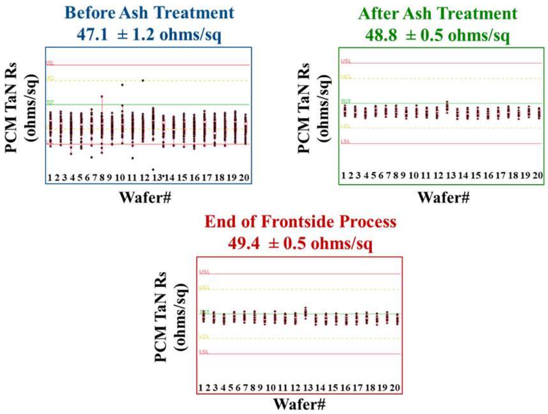

Fig. 8. The downstream ash treatment during M1 stage of the fabrication flow tightened the PCM TaN R_s distribution by 58% and promoted greater thin film stability.

Ultimately, improving the process monitoring scheme through optimization of the FDC system and shorter feedback loop reduced process variation and improved yield. Tracking the progress over an extended period revealed that the distribution of the critical PCM resistor value for a specific resistor dimension of a few microns width that is used to track the integrity of the resistor process was tightened by 25% as depicted in Figure 9. This also improved the process control over both the intra-wafer uniformity and run-to-run uniformity of the deposited TaN thin film. The uniformity and distribution of the intra-wafer R_s measurements were improved by approximately 25% and 54% respectively.

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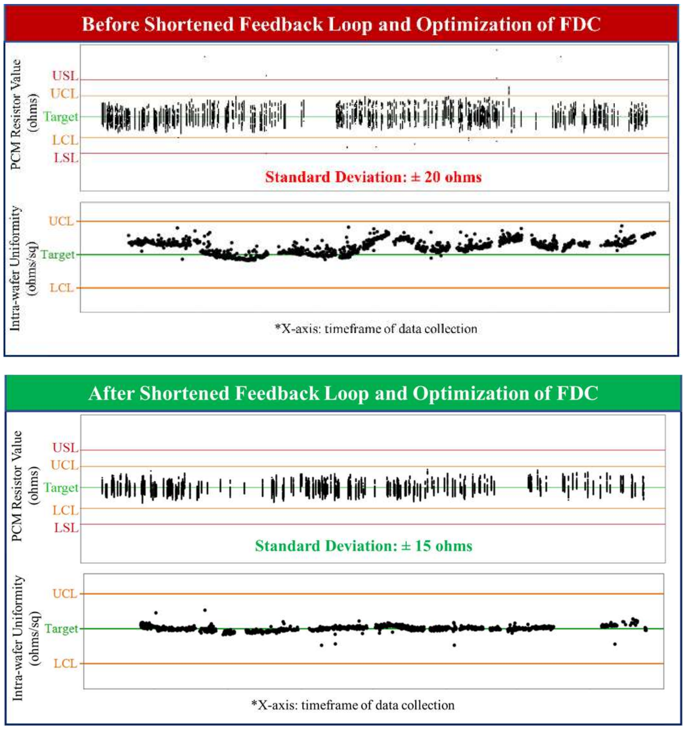


Fig. 9. Deployment of FDC monitoring and the implementation of the short loop sampling plan (M1TEST) tightened the PCM resistor data and thin film uniformity.

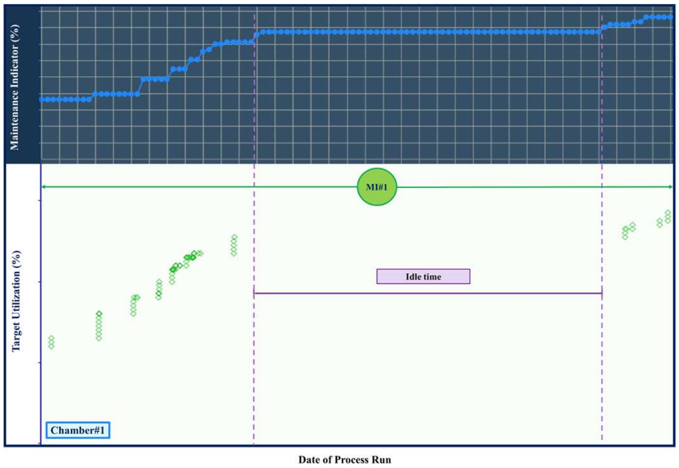
B. Automated Predictive Scheduler for Preventative Maintenance

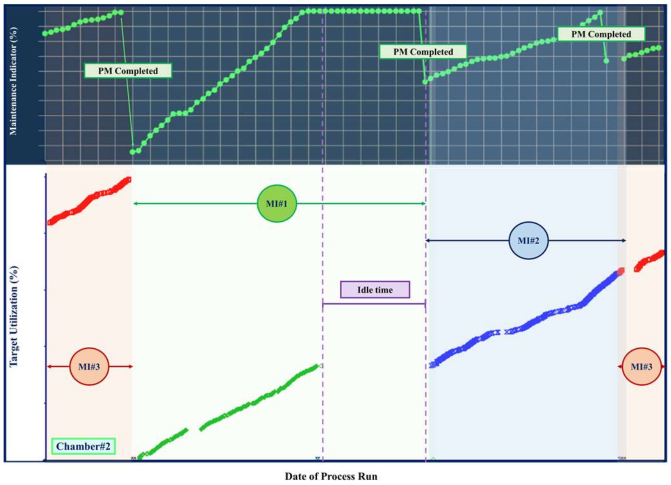
While some cases of parameter excursions detected by FDC arose from process variation or drifts, other cases aligned with approaching maintenance timelines. Reassessing the condition of the sputtering chamber (e.g., outgassing of tooling components, leak rates, cryopump regeneration, bake-out) and equipment parts (e.g., anode ring, shielding, shutter blade) is imperative to maximize process stability and repeatability. Performing PM on a scheduled routine basis is pertinent for extending the Ta target life cycle, reducing equipment failure, increasing cost savings since Ta is a semi-precious metal, and maintaining low defect levels.

For maintenance management, kWh-based target utilization percentages were automatically tracked by MI reports to alarm when the warning thresholds were reached. Threshold limits within these reports were set based on the historical target utilization percentage reached when there was severe degradation of the thin film uniformity.

As shown in Figure 10, MI were set up for different threshold limits, each of which corresponded to completing a specific type of PM; this was based on how far along the Ta target material had been consumed. The software's algorithm fits a line through the acquired data to make a robust prediction on when the threshold limit would be reached. This forecasting method helped to gauge when maintenance activities should be performed or safely postponed without risking product quality. Dedicating time for performing PM reduced unscheduled equipment downtime and the risks of overloaded shielding or burning through the Ta target into the backing plate.

Additional reports were set up to track the chemical consumption for the TaN reactive sputtering process. For instance, monitoring the usage rate of process gases aided the scheduling of facility work to order chemicals and have them readily installed for production usage. Moreover, unexpected upticks in the consumption rate would flag in the report to allow for further investigation to determine the source of these anomalies. Drifts in process trends and inline SPC data would also be thoroughly reviewed to ensure that the product wafers processed during that timeframe remained unaffected.





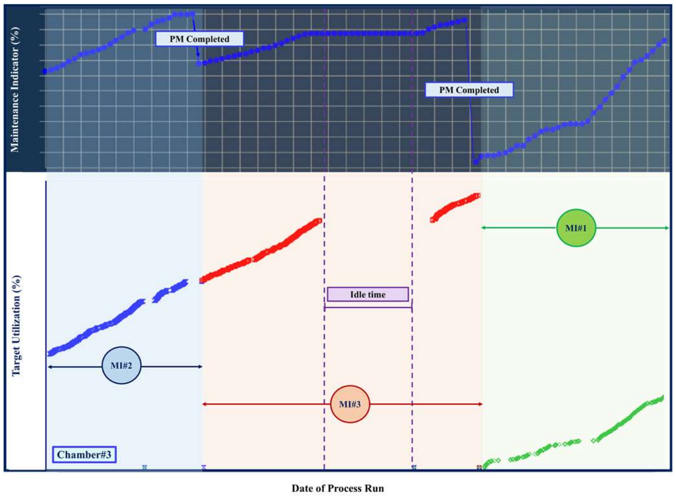


Fig. 10. Time series plots of the maintenance indicators' progression toward the specified threshold limits for three sputtering chambers at different stages of their Ta targets' life cycles. A stagnant maintenance indicator's percentage would indicate that the tool was idled during that timeframe.

C. Customization of Process Monitoring Reports and Models

Performing analyses at multiple levels maximized the automated detection of a variety of process faults. This identified areas that needed improvement with optimized tool capabilities for the TaN reactive sputtering process. The customizability of the filtered model type allows for tracking of statistical calculations that are most suited for each process parameter. While some reports have user-defined control limits, other reports have limits determined by evaluating the historical trends for each process chamber or recipe. For instance, the recipes used for conditioning the Ta target to remove surface contamination after PM reach higher platen temperatures than standard production recipes. The FDC's history splitting feature by recipe tracks the platen temperature for each process recipe based on its own historical target and trends. Platen heating by lamp radiation is used for degassing wafers of impurities, such as water moisture and nitrogen gas. Implementation of real-time process monitoring with interdiction capabilities flagged the conditioning runs that had OOC platen temperatures. This reduced the quantity of "burnt" or warped monitoring wafers in Figure 11 that resulted in aborted process runs due to the tool's handling issues. The detectability of fluctuations in the platen temperature was further enhanced by setting up FDC reports that captured additional statistical calculations beyond the single point readout of the platen temperature for each wafer run.

The automated history reset is another helpful feature that was configured to reset the historical calculations of a report when an expected change to the process or equipment takes place. For instance, after PM procedures are completed for replacing a Ta target, there is often a notable shift in the figure of merit (FOM), voltage, as shown in Figure 12. However, this is not surprising since the deposition power and time are adjusted at larger increments to retarget the inline R_s and account for the distance between the thicker, newly installed Ta target and the substrate. Moreover, the chamber requires time to stabilize after being vented and conditioned. The change in impedance as seen by the radio frequency (RF) generator and matching network of the sputtering chamber also contributes toward the expected shift in voltage. Therefore, the FDC report used to track voltage is configured such that its SPC history will reset when there is a decrease in the target utilization percentage, which signifies that the Ta target has been replaced.

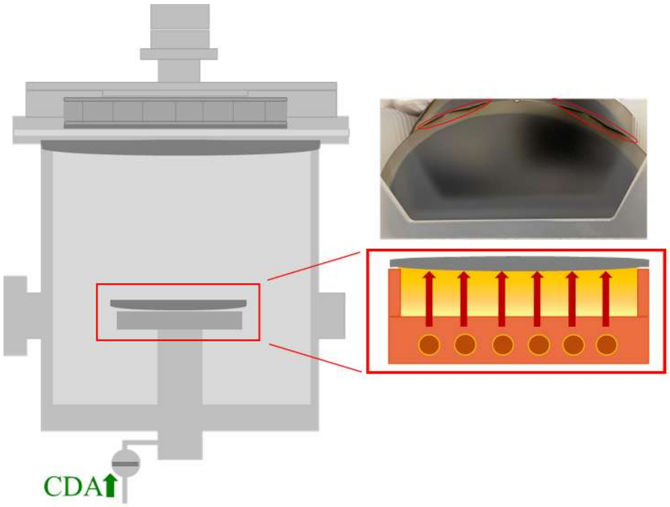


Fig. 11. The wafer's temperature during the deposition process is influenced by platen heating which occurs through lamp radiation. Silicon monitoring wafers that were repeatedly used to condition the Ta target had a visible "burnt" outer ring due to higher platen temperatures.

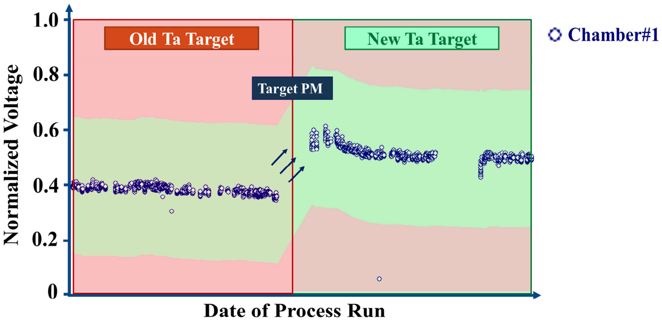


Fig. 12. An expected shift in voltage is detected during the process runs after a Ta target had been newly installed in the sputtering chamber.

D. Recipe Management System and Process Capability Timers

The system's tool recipe verification system compares the current recipes against their respective golden recipes at a set time interval and flags for mismatched parameters as shown in Figure 13. Tool interdiction would prevent lots from being processed with a corrupted process recipe, ensuring that all wafers are being processed with the intended values for each recipe parameter.

Capability timers were also implemented using EPI SPC reports to automatically switch off access to process recipes that required requalification. For instance, reload recipes are used during the events of high work-in-progress (WIP) at the resistor layer deposition step. The recipe parameters are set up such that the inline TaN R_s will remain stable even if wafers are processed in the same sputtering chamber without satisfying the

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minimum tool idle time between cassette-to-cassette runs required by the standard production recipe. Detection of OOC inline TaN data would disqualify the reload recipe and signal for recipe adjustments to be made to retarget the R_s.

In alternative scenarios, certain devices with unique process specifications require a different targeted inline R_s. These nonstandard recipes are set up with different values for deposition time and power to achieve the custom TaN thin film R_s. A timer would be automatically initiated by the system when the EPI SPC report detected a wafer being processed with a nonstandard recipe. As shown in Figure 14, process capabilities that corresponded to these nonstandard recipes would be automatically switched off by the system's capability timers when they were not run for an extended period, thereby preventing the accidental selection of unqualified recipes and minimizing the risk of misprocessed wafers.

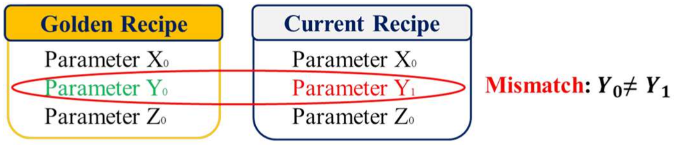

Fig. 13. The recipe verification system through FDC compares each of the equipment and process parameters between the golden and current recipes to detect and flag for mismatches.

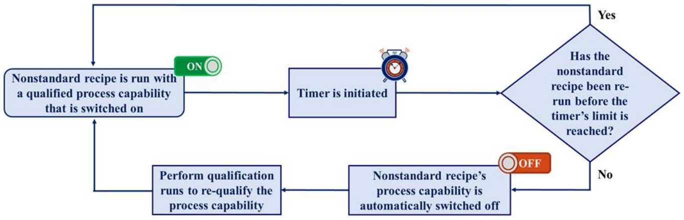

Fig. 14. Flow chart of automatic toggling of process capabilities for nonstandard TaN deposition recipes based on their qualified status.

F. Process Tracking and Utilization

The tracking and utilization summary reports aided the strategic usage of the process chambers in production to maximize throughput while abiding by process requirements. For instance, there is a minimum idle time between cassette-to-cassette runs for the standard production recipe to allot time for chamber stabilization.

The process coverage key performance indicator (KPI) provided insight on the percentage of processes being monitored by at least one analysis. Figure 15's time series plot shows the percentage of time each sputtering chamber spent in acquisition states that correspond to running specific recipes as opposed to remaining idle. The number of wafers processed in each sputtering chamber is tracked as the process count in Figure 16. This provides a summarized analysis to gauge the flow of WIP that progresses through the resistor layer sputter deposition step.

Utilization reports such as the one shown in Figure 17 provided greater visibility of when chambers are actively processing wafers. Determining that there were no FDC process excursions or anomalies in inline SPC allowed for the qualified release of simultaneously processing wafers with the standard production recipe in two separate sputtering chambers from the same tool platform as shown in Figure 18. This not only doubled the throughput at the resistor layer deposition step but also increased the flexibility of scheduling and performing PM on the sputtering chambers. This further minimized the risks of facing bottlenecks in the production environment for events of high WIP.

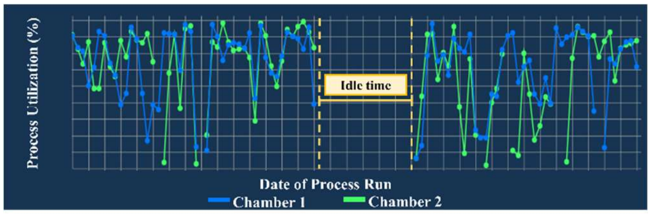

Fig. 15. Time series plot of the process utilization for each sputtering chamber

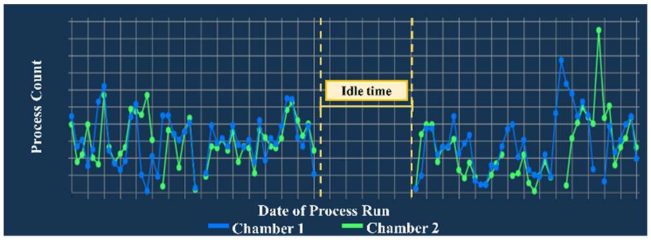

Fig. 16. Time series plot of the process count for each sputtering chamber

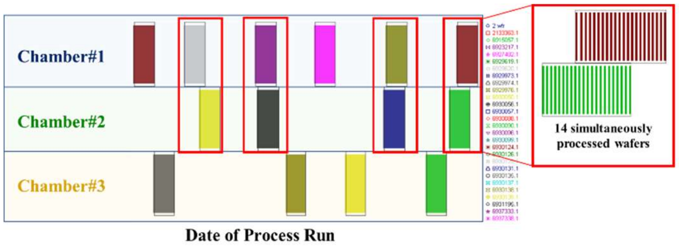

Fig. 17. The process tracking and utilization report allows for monitoring of each sputtering chamber's activity. Boxed in red are pairs of simultaneously processed runs.

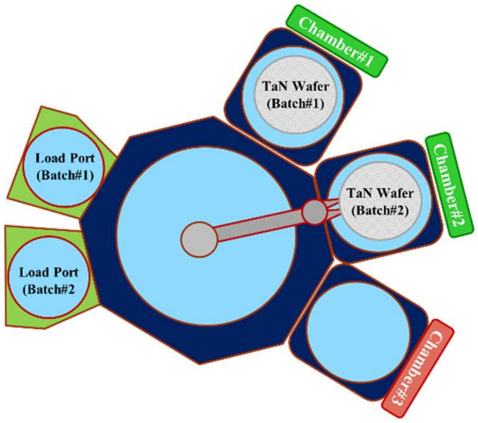

Fig. 18. Two sputtering chambers from the same tool module are simultaneously processing wafers from batch#1 and batch#2.

IV. CONCLUSION

Engineering analytical tools and machine learning were integrated within the third-party FDC system to perform automated training, create statistical predictive models, and summary reports for analyzing tool health and process metrics. The effective use of predictive maintenance scheduling has improved the line balance at the resistor layer stage and ensured a timely reassessment of chamber conditions to sustain the quality of the sputtered thin films. Furthermore, the risk of misprocessed wafers and wafer scrap was significantly reduced through the implementation of automated process capability timers and a central recipe management system.

The simplified deployment of this robust automated process monitoring scheme has strengthened the detectability of process drifts and excursions at earlier steps within the fabrication flow. With the enhanced process visibility through data visualization and automated statistical analysis, accurate correlations can be drawn between inline SPC for TaN thin film characterization and the monitored process parameters. Optimizing FDC capabilities along with implementing a short loop sampling plan for FDC-flagged wafer runs not only tightened the distribution and improved the targeting of critical TaN PCM resistor parameters, but also improved the run-to-run and intra-wafer thin film uniformity. Ultimately, improving the quality control over the device fabrication through prevention and detection of process anomalies minimized product defects and variation for the TaN TFR. Establishing tighter control over the manufacturing variation opens opportunities for competitive designs that may have tighter tolerances in product specifications but can substantially improve the resistor performance.

While this study examined the implementation of an enhanced FDC system to monitor and optimize the TaN TFR process, the methodologies discussed can be applied to a wide variety of semiconductor materials. Strategies described for process monitoring are also applicable beyond sputter deposition to other methods of thin film deposition. Additional areas of device fabrication in semiconductor manufacturing processes, such as etching and photolithography, can adopt and implement these techniques to minimize the risk of wafer scrap, improve product quality, and reduce production costs.

ACKNOWLEDGMENT

The authors would like to acknowledge the contributions from colleagues across various cross-functional teams at Skyworks Solutions for their support to optimize the TaN TFR performance and strengthen the prevention and detection of process drifts in the fabrication flow through the implementation of a robust FDC system. Special thanks to Nercy Ebrahimi for his support as well as Ravi Ramanathan for his feedback and manuscript review.

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