INTERNATIONAL TELECOMMUNICATION UNION

TELECOMMUNICATION STANDARDIZATION SECTOR

STUDY PERIOD 2022-2024

SG15-C-0319

STUDY GROUP 15

Original: English

Question(s): [13/15] [Geneva, 17-28 APR 2023]

CONTRIBUTION

Source: Skyworks Solutions Inc

Title: Extended QL TLV Handling Correction within G.8264

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Abstract: It proposes modification on the extended QL TLV handling within G.8264, in particularly, the specification from clause 11.3.1.4 for the interworking between different SyncE generations for the intermittent EEC node, that is capable to handle the extended QL TLV.

Introduction

The authors acknowledge the benefits from discussion with Skyworks colleague Michal Fakhry.

As G.8264 [ref 1], the extended TLV for transmitting enhanced QL is defined in the table 11-5.

The bit[0] of Flag field indicating if there is mixed EEC and eEEC chain. 0 if all the clocks are eEEC, and 1 if at least one of the clocks is NOT an eEEC.

The bit[1] of Flag field indicating if the chain is completed or partially. 1 if the TLV has been generated in the middle of the chain and the count of EEC/eEEC is partial, and 0 if the count is completed for all the nodes.

In the clause of 11.3.1.4, it specifies how the bit[0] and bit[1] being handled under various cases, and at the end, as the highlighted paragraph copied below, it is NOT correct and does not reflect the purpose and the usage of bit[1]. This contribution goes through analysis of various cases and proposes changes of handling of bit[1].

---------- below is related information copied from current G.8264 ------

Table 11-5 – Extended QL TLV

Octet number	Size/bits	Field
1	8 bits	Type: 0x02
2-3	16 bits	Length: 0x0014
4	8 bits	Enhanced SSM code (see Table 11-6)

5-12	64 bits	SyncE clockIdentity of the originator of the extended QL TLV (Note 1)
13	8 bits	Flag (Note 2)
14	8 bits	Number of cascaded eEECs from the nearest SSU/PRC/ePRC
15	8 bits	Number of cascaded EECs from the nearest SSU/PRC/ePRC
16-20	40 bits	Reserved for future use
NOTE 1 – The synchronous Ethernet (SyncE) clockIdentity is formatted as per this clause. The originator of the extended QL TLV refers to the clock that starts or restarts the counts of cascaded clocks within the TLV. If the count of clocks is started or restarted in the middle of the chain, the partial chain bit is set to 1 (see Note 2 and clause 11.3.1.4). NOTE 2 – Bit 0 means mixed EEC/eEEC (i.e., 1 if at least one of the clocks is not an eEEC; 0 if all clocks are eEEC); bit 1 means partial chain (i.e., 1, if the TLV has been generated in the middle of the chain and the count of the EEC/eEEC is incomplete); bits 2-7 reserved for future use. See also clause 11.3.1.4.		

11.3.1.4 Interworking between different SyncE generations

While the extended QL TLV was developed for use with the eEEC, the basic mechanism could be applied in the future to the older EEC. This results in three possible combinations of clocks that need to be considered; eEEC with extended QL TLV support, EEC with no extended QL TLV support, and EEC with extended QL TLV support.

In case of already deployed nodes not supporting the extended QL TLV, interworking between different generations of synchronous Ethernet is achieved by the fact that a network element must discard and not forward upon reception any TLV within the ESMC PDU that it does not recognize.

The extended QL TLV allows the count of the number of cascaded eEEC and EEC clocks. If a clock not supporting the extended QL TLV is present within a chain of clocks, discarding the TLV, as noted above, will result in incomplete counts. The extended QL TLV specifies a flag to allow clocks supporting enhanced ESMC messages to have the ability to report the presence of clocks that may have discarded TLVs.

As an example, in case of a chain of eEECs, bit 0 and bit 1 will both be "0" at the output of the chain indicating that the syncE chain is fully based on eEECs, and the count of clocks is complete.

In case of an intermediate EEC, not able to process the extended QL TLV, the EEC shall drop the TLV. At the next eEEC in the SyncE chain, the TLV will be added with both bit 0 and bit 1 set to "1" to indicate that the SyncE chain is not fully based on eEEC, and the count of clocks is not complete.

However, in case of an intermediate EEC that is able to process the extended QL TLV, at the output of that EEC bit 0 is set to 1 to indicate that the SyncE chain includes a mix of EEC and eEEC, and bit 1 is set to 0 to indicate that the count of the clocks in the chain is complete.

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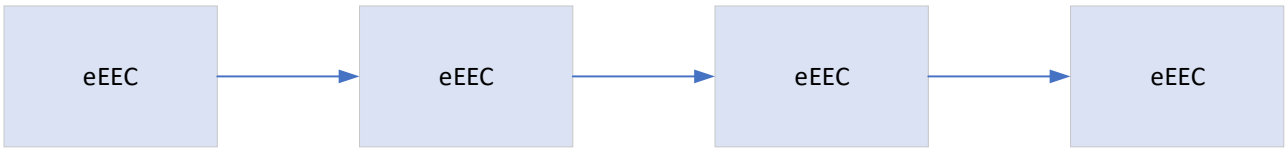
Discussion

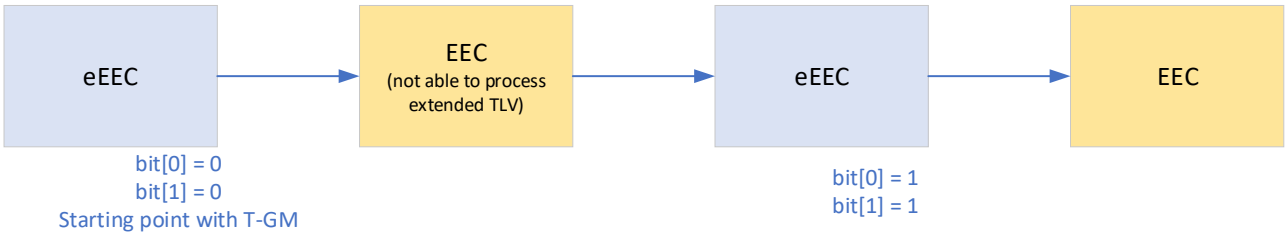
Here are various use cases.

(1) Full chain with eEEC: current specification is accurate.



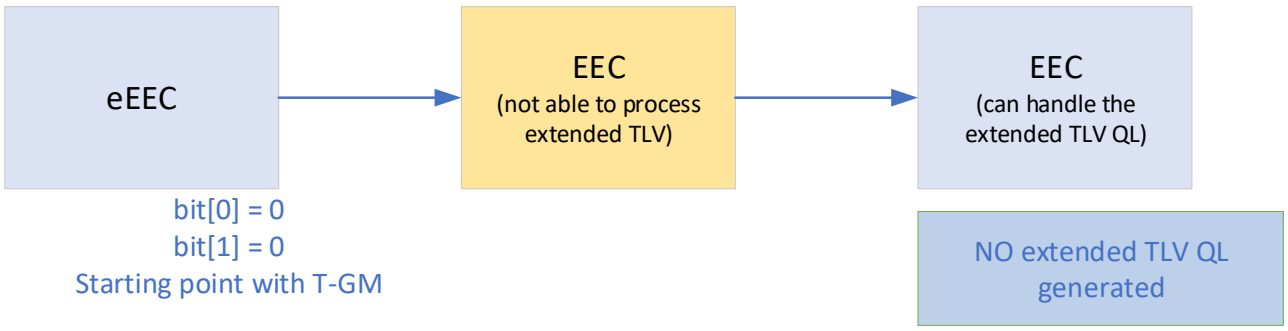
"As an example, in case of a chain of eEECs, bit 0 and bit 1 will both be "0" at the output of the chain indicating that the syncE chain is fully based on eEECs, and the count of clocks is complete"

(2) Mixed but EEC discard extended QL TLV: current specification is accurate.



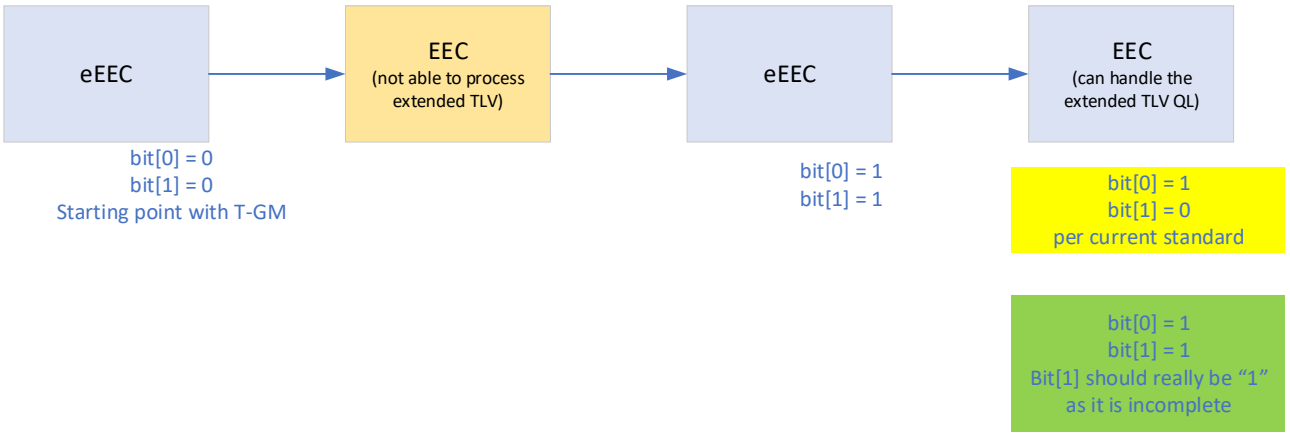
"In case of an intermediate EEC, not able to process the extended QL TLV, the EEC shall drop the TLV. At the next eEEC in the SyncE chain, the TLV will be added with both bit 0 and bit 1 set to "1" to indicate that the SyncE chain is not fully based on eEEC, and the count of clocks is not complete"

(3) Mixed but previous EEC dropped extended TLV: no specification on if extended TLV QL being generated or not.



In this case, even second EEC can handle extended TLV QL, but it does not receive, and no need to generate extended TLV QL.
If indeed, the new extended TLV QL being generated, both bit 0 and bit 1 should set to "1".
The current standard has no specification on it.

(4) Mixed but one EEC discard extended QL, and another EEC can handle extended QL and extended TLV received – current specification is NOT correct.



The current specification is not correct on the bit[1] handling.

"However, in case of an intermediate EEC that is able to process the extended QL TLV, at the output of that EEC bit 0 is set to 1 to indicate that the SyncE chain includes a mix of EEC and eEEC, and bit 1 is set to 0 to indicate that the count of the clocks in the chain is complete."

- From this specification of text, the last EEC should set bit[0] = 1, which is correct. Then it requires to set bit[1] = "0" which is not correct, as the chain is not completed and the first EEC drops extended TLV.
- The second EEC does not really have information if it is completed or not, the logic way is for it to pass the bit[1] value from it receives to the output. Therefore bit[1] should be "1" as it receives "1", and bit[1] should be "0" if it receives "0".

Proposal

From above analysis, combining the use case 3 and use case 4, it proposes changing the paragraph from:

"However, in case of an intermediate EEC that is able to process the extended QL TLV, at the output of that EEC bit 0 is set to 1 to indicate that the SyncE chain includes a mix of EEC and eEEC, and bit 1 is set to 0 to indicate that the count of the clocks in the chain is complete."

To:

"However, in case of an intermediate EEC that is able to process the extended QL TLV, at the output of that EEC bit 0 is set to 1 to indicate that the SyncE chain includes a mix of EEC and eEEC, and bit 1 is set to the value whichever it receives. When no extended QL TLV received, it will be regular EEC and no extended QL TLV output generated."

Alternative proposal is to generate the extended QL TLV output when no extended QL TLV is received.

"However, in case of an intermediate EEC that is able to process the extended QL TLV, at the output of that EEC bit 0 is set to 1 to indicate that the SyncE chain includes a mix of EEC and eEEC, and bit 1 is set to the value whichever it receives. When no extended QL TLV received, both bit 0 and bit 1 are set to 1 for extended QL TLV output"

References

[1] ITU-T, G.8264, Distribution of timing information through packet networks, 03/2018