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Process Optimization of Rapid Thermal Alloyed Collector Metal Layer in Compound Semiconductor Devices

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Abstract

This paper discusses the optimization of the critical collector contact (CC) in compound semiconductor devices. It also addresses solutions to fundamental challenges including a robust procedure for detecting and minimizing process variation and drifts in the high-volume manufacturing environment. While insufficient alloying results in an incompletely formed collector contact, excessively high temperatures during or downstream from the alloy step results in undesirable diffusion. Run-to-run process variation was minimized, and intra-wafer heating uniformity was improved through dialing in the rapid thermal alloy process recipe and temperature profile as well as utilizing graphite susceptors for identical backside conditions for wafer processing. Implementation of a short loop for earlier electrical testing of collector parameters on process control monitor (PCM) structures after downstream oxidative and thermal treatments in the device fabrication flow had reduced the standard turnaround time by an average of 35%. This not only expedited recipe qualification procedures at a time-sensitive step but also enhanced statistical process control for production. As such, low collector contact resistance (R_C) was achieved; hence series resistance and impedance into the device were reduced.

Keywords

Alloy, Collector contact, Resistance, Gallium arsenide, Statistical process control

Introduction

In our compound semiconductor devices, the ohmic contact is defined as the low resistance semiconductor junction between the metal and gallium arsenide (GaAs) substrate with a linear relationship between voltage to current. The critical ohmic contact within our heterojunction bipolar transistor process is the CC established through the metal deposition and the rapid thermal alloy process [1].

Materials and Methods

Method for measuring TLM and split collector structures

Measurements of both the transmission line model (TLM) and split collector structures for inline electrical characterization provided an early evaluation of the semiconductor device performance in heterojunction bipolar transistor processing. The collector split resistance is used as a PCM test for measuring the collector R_C and epitaxial sheet resistance (R_S); its sensitivity to variation in the collector is especially critical for ensuring high reproducibility of smaller features [2]. In the TLM measurement, current is passed through the metal pads and the

resulting voltage drop is measured to calculate the resistance.

Method for defect detection on CC structures

In addition to electrical testing of the collector or ohmic contact resistance, routine inspection of the surface morphology was conducted to survey the CC structures for any defects.

Previous studies were conducted to assess the effects of different wet chemicals used in surface preparation and etching processes to minimize or eliminate the risk of GaAs corrosion. Corrosion between the interface of the metal and exposed GaAs, for devices with small ohmic contacts, inhibit the flexibility of designs that aim for shrinking the die size [3]. Furthermore, minimizing the duration of exposed CC structures during subsequent processing is crucial to prevent blistering.

Materials and methods to deposit and alloy CC metal stack

In this study, rapid thermal processing was conducted to alloy the evaporated metal stack of approximately 200 nm thickness at the eutectic temperature to achieve low collector R_C for the compound semiconductor device. The deposited CC metal stack shown in figure 1 is comprised of gold germanium (AuGe), nickel (Ni), and gold (Au). The low eutectic temperature of AuGe allows for sufficient alloying of the CC metal stack without disturbing the epitaxial layers below. Ni acts as a wetting agent for aiding the diffusion of Au and AuGe. Au allows for the out-diffusion of gallium (Ga) and minimizes the resistance introduced through the fabrication process itself; this is favorable for designers since it enables greater controllability over the total resistance. Alloying the metal stack creates the critical collector and ohmic contacts, allowing the displacement of Ga atoms with Ge atoms with the aim of achieving low collector R_C [4].

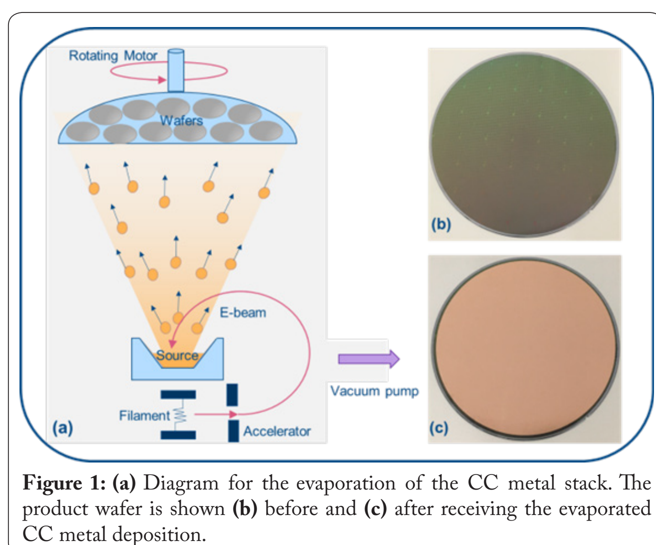

Figure 1: (a) Diagram for the evaporation of the CC metal stack. The product wafer is shown **(b)** before and **(c)** after receiving the evaporated CC metal deposition.

Results and Discussion

Optimizing the alloy temperature profile and minimizing process variation

Dual side heating lamps shown in figure 2 allowed for greater heating uniformity and reduced risk for wafer warpage. Various parameters, such as the intervals of process time,

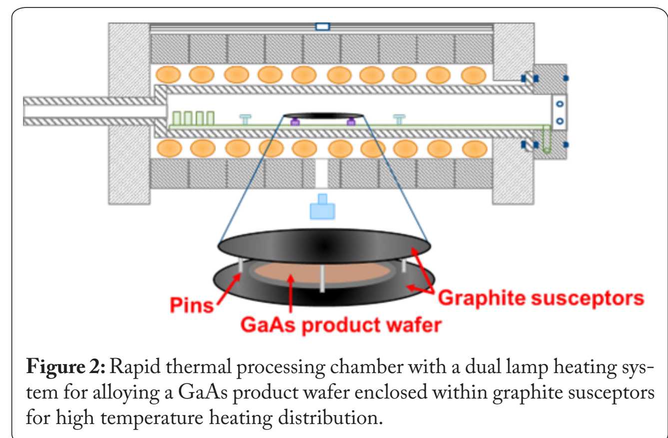

Figure 2: Rapid thermal processing chamber with a dual lamp heating system for alloying a GaAs product wafer enclosed within graphite susceptors for high temperature heating distribution.

power, temperature, and gas flow rates are critical parameters that were fine-tuned at each process step to achieve a temperature profile adequate for alloying the CC metal stack; this evaluation was verified through electrical characterization of PCM structures.

As shown in figure 3, a series of ramps and stabilization steps were used to construct the temperature profile for rapid thermal alloying. Misalignment or topology of patterned wafers may result in an uneven heating distribution. The temperature profile of a batch process' first wafer may also slightly vary due to the quartz chamber's differing heat capacity and initial temperature after extended tool idle time. The addition of a preheating step, pre-aligner for consistent wafer orientation and position, as well as the utilization of graphite susceptors for identical backside conditions during wafer processing facilitated a more consistent run-to-run temperature profile and uniform heating distribution. Although the temperature profile of the first wafer in a batch may slightly differ, electrical characterization of the inline TLM R_C and CC parameters after optimized conditioning of the chamber provided verification that the effect on electrical performance was minimal. Utilizing the infrared camera to study the thermal distribution induced by the rapid thermal process as depicted in figure 4 provided greater insight into how different backside conditions of the wafer and susceptor can significantly vary the temperature profile and heating uniformity.

Assessment of downstream effects on CC parameters

To study the downstream effects on electrical characterization of the collector layer, PCM structures were measured for collector R_C after oxidative and thermal processes that

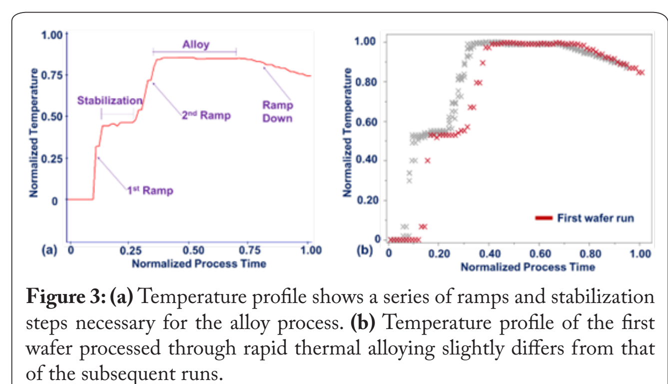

Figure 3: (a) Temperature profile shows a series of ramps and stabilization steps necessary for the alloy process. **(b)** Temperature profile of the first wafer processed through rapid thermal alloying slightly differs from that of the subsequent runs.

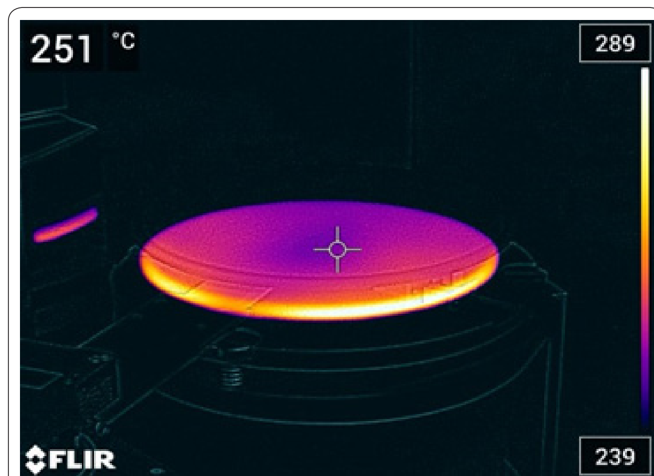

Figure 4: Temperature distribution map of the graphite susceptor with an enclosed GaAs product wafer after exiting the quartz furnace for cool down in the ambient environment.

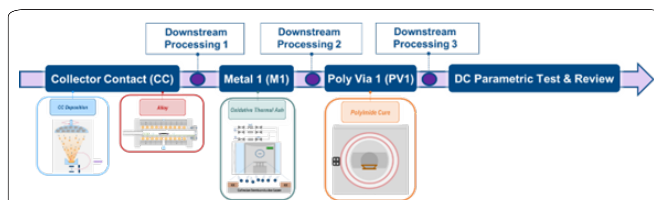

Figure 5: Both oxidative and thermal downstream processes were assessed for their impact on CC parameters from the CC stage to the end of frontside processing where direct current parametric test and review takes place.

were downstream from the CC stage, as shown in figure 5. Performing electrical testing at various steps of the device fabrication allowed for (1) establishing a short loop at Poly Via (PV1) stage for collector PCM data comparable to the end of frontside process as well as (2) enhancing the detectability and understanding of how the process data shifts throughout the fabrication flow.

In particular, this provided crucial insight into the response of collector R_C to oxidative and thermal processes that are expected to cause the greatest shift, namely the oxidative thermal ash treatment at Metal 1 (M1) stage in figure 6 and high thermal treatment through poly cure at PV1 in figure 7. As shown in figure 8, this revealed a minimal shift in average collector R_C of 3.24E-3 ohm-mm between PV1 and the end-of-frontside device process. As such, strengthened detectability measures of process variation can significantly reduce wafer scrap arising from process drifts. A short loop shown in figure 9 was established for electrical testing of collector parameters with an effective reduction in average turnaround time for feedback by 35%.

The implementation of this short loop for electrical characterization resulted in copious benefits. For instance, after invasive preventative maintenance, the rapid thermal processing tool and process recipe must be requalified for production usage. Expedited electrical characterization prevented production schedule delay and bottleneck situations in the high-volume manufacturing environment; this is especially critical since the CC layer has stringent coupling times in which certain steps are time-sensitive to minimize moisture ingression that arises from prolonged exposure to ambient environmental conditions. Furthermore, yield investigations for root cause analysis of electrical failures can be effectively troubleshot by narrowing down the processes downstream from the CC stage in the fabrication process flow to pinpoint sources of these issues.

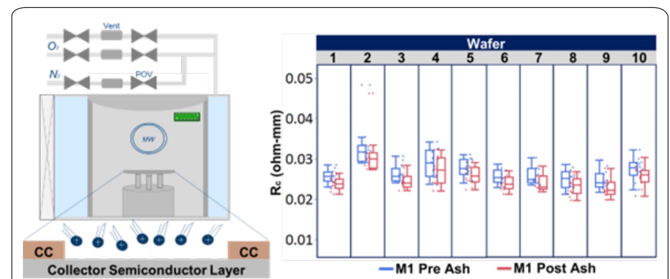

Figure 6: Oxidative and highly thermal ash treatment removes resist residues after M1 deposition and lift-off, resulting in a downward shift of average collector R_C by -1.79E-3 ohm-mm.

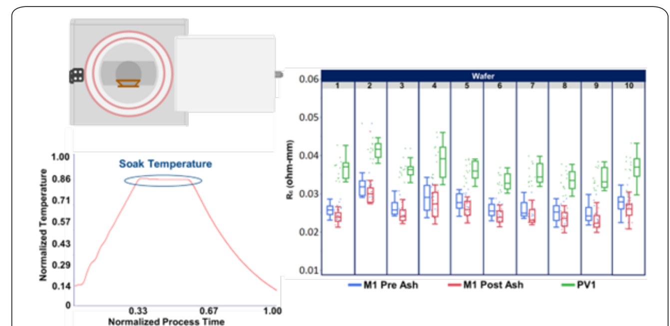

Figure 7: Downstream thermal treatment during polyimide cure results in an upward shift for collector R_C by 1.11E-2 ohm-mm.

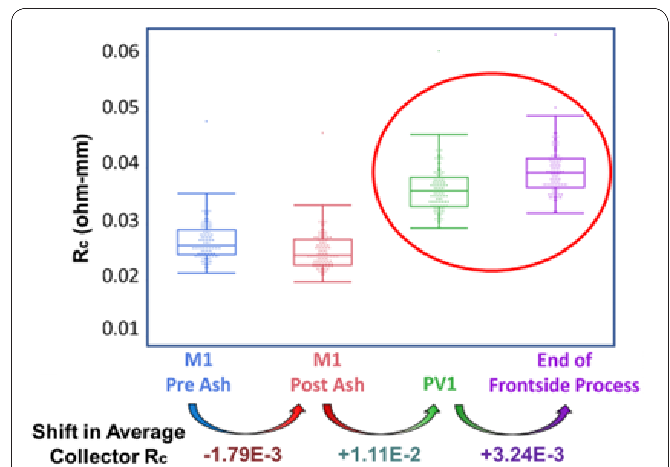

Figure 8: Progression of collector R_C measured at several stages downstream from the alloy step: M1, PV1, and end of frontside process. Minimal shift in average collector R_C between PV1 and end of frontside process allows for early electrical characterization of collector-related parameters.

Root cause analysis for significant yield loss of high collector split resistance and CC resistance

The shorter feedback loop as discussed above provides important insight into what collector values are expected at different steps in the fabrication flow (e.g., M1 and PV1) for

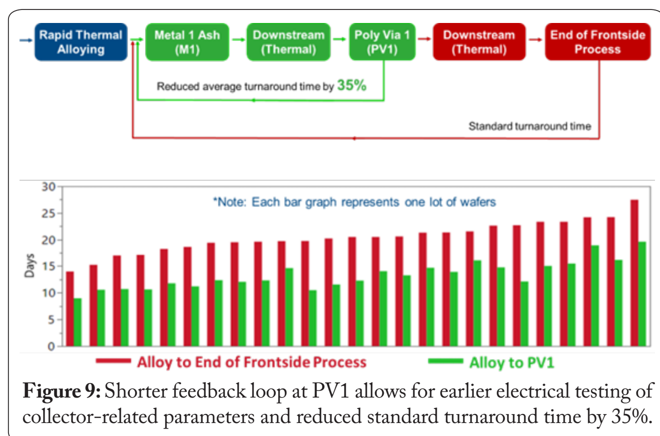

Figure 9: Shorter feedback loop at PV1 allows for earlier electrical testing of collector-related parameters and reduced standard turnaround time by 35%.

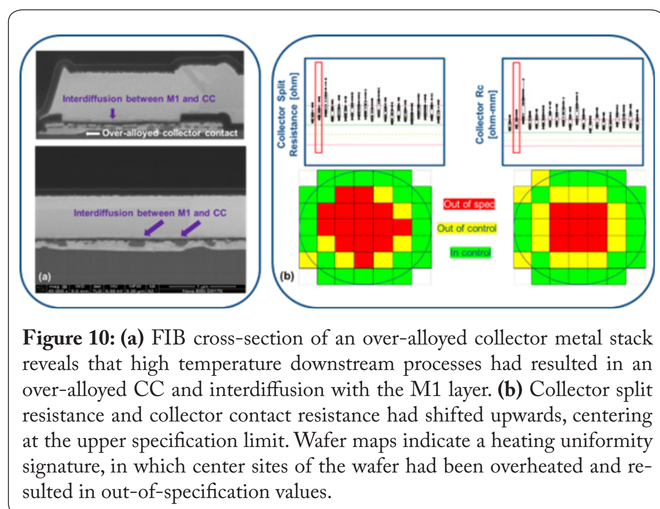

Figure 10: (a) FIB cross-section of an over-alloyed collector metal stack reveals that high temperature downstream processes had resulted in an over-alloyed CC and interdiffusion with the M1 layer. **(b)** Collector split resistance and collector contact resistance had shifted upwards, centering at the upper specification limit. Wafer maps indicate a heating uniformity signature, in which center sites of the wafer had been overheated and resulted in out-of-specification values.

nominal versus over-alloyed conditions. In the case study shown in figure 10, the focused ion beam (FIB) cross-section of an over-alloyed collector metal stack revealed that a highly thermal downstream process resulted in interdiffusion between the CC and M1 layer. This led to the collector split resistance and collector R_C being out-of-specification. Correlating the wafer maps of collector electrical parameters to the temperature uniformity expected at different process steps provided greater insight into whether the poorly yielding sites were attributed to a known uniformity signature.

Minimizing the risk of blisters and defects at the process-sensitive CC stage

In general, there are two common categories of blister defects found on the CC PCM and device structures: (1) moisture-induced blisters in figure 11 and (2) repeating "dot-like" pre-clean-induced blisters in figure 12. These blistering signatures can be characterized at varying severities.

For moisture-induced blisters, less severe defects can be detected on the surface of CC structures while moderately severe defects often emerge as bubbles along the edges of these structures. Blisters of greater severity can lead to yield loss due to failing electrical measurements for PCM parameters; a sample FIB cross-section of such a defect is shown in figure 13. Extensively long queue times both before and after alloy can result in severe blistering on the CC structures. Since the blister effect is additive, vigilant discipline in abiding by close coupling times is crucial to minimize the contact exposure to ambient conditions.

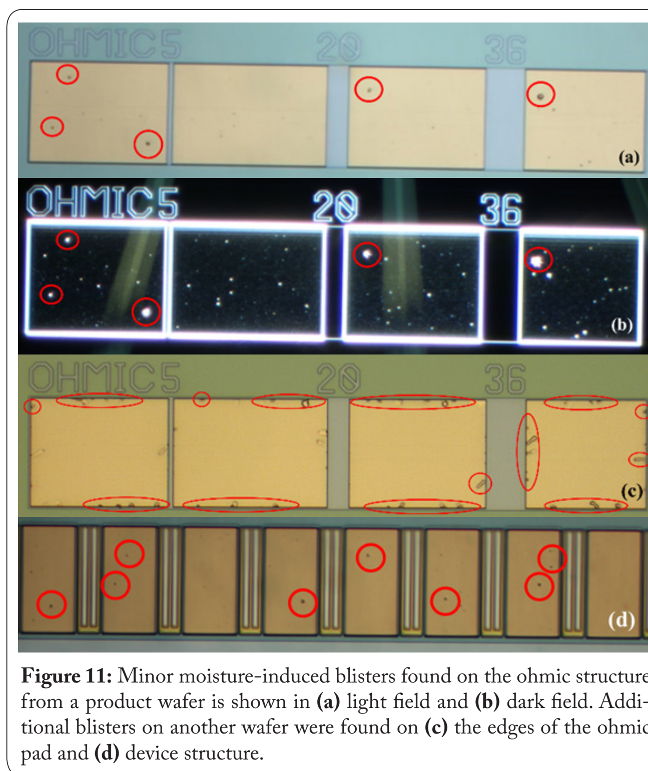

Figure 11: Minor moisture-induced blisters found on the ohmic structure from a product wafer is shown in **(a)** light field and **(b)** dark field. Additional blisters on another wafer were found on **(c)** the edges of the ohmic pad and **(d)** device structure.

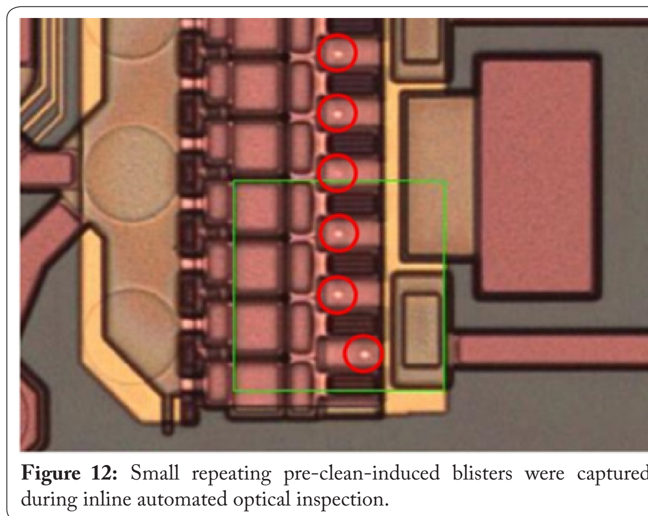

Figure 12: Small repeating pre-clean-induced blisters were captured during inline automated optical inspection.

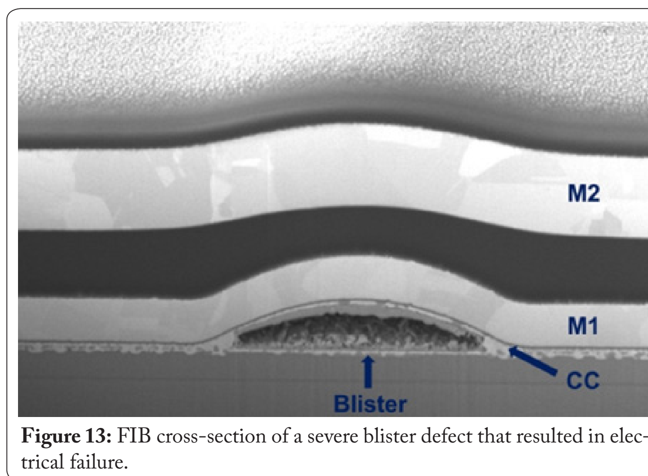

Figure 13: FIB cross-section of a severe blister defect that resulted in electrical failure.

After the alloy stage, wafers undergo additional processing in the device fabrication. Further downstream, M1 is evaporated. This deposited metal layer seals the collector contacts, extensively minimizing the risk of further blistering on the CC layer. Therefore, reducing the work-in-progress of wafers queued at the CC stage at a given time is crucial for preserving the quality and integrity of these devices.

By comparison, smaller repeating blisters associated with the pre-clean are variable in size, localized on the wafer, and generally form a pattern on specific collector structures. These defects were caught during inline inspection and flagged for dispositioning to determine yield loss through automated optical inspection as shown in figure 14. Unlike the moisture-induced blisters that frequently appeared on the ohmic structures, these "dot-like" pre-clean-induced blisters were not apparent on these structures as shown in figure 15. The FIB cross-section in figure 16 was performed after CC metal deposition and prior to alloying, revealing the severity of the pre-clean-induced blister.

Conclusion

The alloy process was optimized and the detectability of downstream effects on CC was enhanced. Tuning in the process recipe and temperature profile for alloying the CC metal stack achieved a low collector R_C to reduce series resistance or impedance into the device. Furthermore, establishing a short loop for testing CC parameters at PV1 allowed for expedited detection of process drifts, recipe and tool requalification, effective yield troubleshooting, and improved SPC. As shown in figure 17, reliability data of GaAs product wafers following PCM testing at the end of the frontside device process for the collector R_C measured before and after the high temperature reliability bake was well within the specification limits. Such results further indicate the robustness and integrity of the optimized collector contact for the compound semiconductor device.

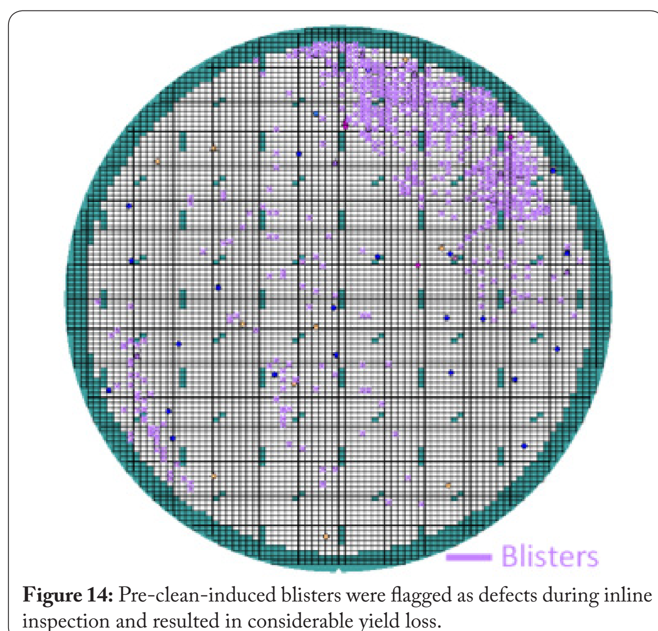

Figure 14: Pre-clean-induced blisters were flagged as defects during inline inspection and resulted in considerable yield loss.

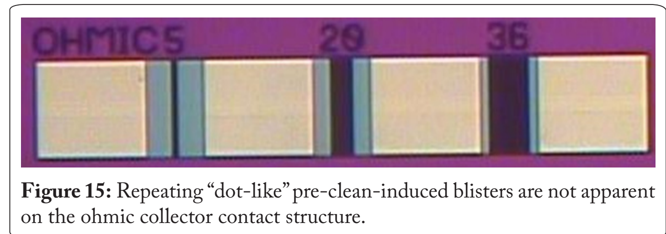

Figure 15: Repeating "dot-like" pre-clean-induced blisters are not apparent on the ohmic collector contact structure.

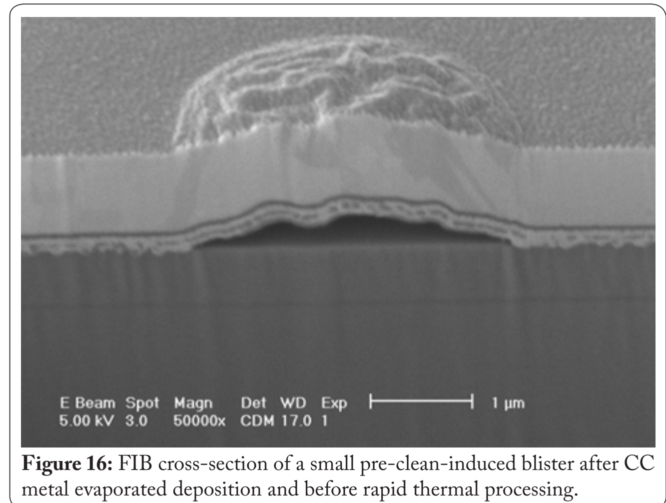

Figure 16: FIB cross-section of a small pre-clean-induced blister after CC metal evaporated deposition and before rapid thermal processing.

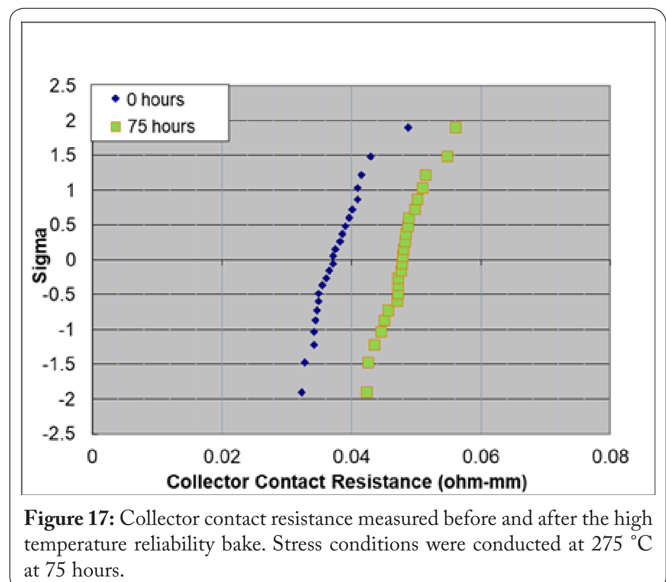

Figure 17: Collector contact resistance measured before and after the high temperature reliability bake. Stress conditions were conducted at 275 °C at 75 hours.

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Conflict of Interest

Authors declare no conflict of interest.

References

1. Li J, Brown T, Janani M, Yota J, Cismaru C, et al. 2016. Challenges for establishing a high volume, high yielding BiHEMT manufacturing process. *International Conference on Compounds Semiconductor Manufacturing Technology (CS MANTECH) Technical Digest pp 41-44.*

2. Luu-Henderson L, Weaver D, Knoedler H, Tiku S. 2011. Collector contact optimization in GaAs HBT manufacturing. *International Conference on Compounds Semiconductor Manufacturing Technology (CS MANTECH) Technical Digest.*

3. Shen H, Luu-Henderson L, O'Neil S, Tiku S, Grayson T, et al. 2004. GaAs corrosion under ohmic contacts by electrochemical oxidation in HBT device fabrication. In *International Conference on Compounds Semiconductor Manufacturing Technology (CS MANTECH) Technical Digest.*

4. Lin HC, Senanayake S, Cheng KY, Hong M, Kwo JR, et al. 2003. Optimization of AuGe-Ni-Au ohmic contacts for GaAs MOSFETs. *IEEE Transactions on Electron Devices* 50(4): 880-885. https://doi.org/10.1109/TED.2003.812097